Product Specifications		
PART NO.:	**VL470L2925-B3SG**	**REV: 1.0**

General Information

1GB 128Mx64 DDR SDRAM NON-ECC UNBUFFERED SODIMM 200-PIN

Description

The VL470L2925 is a 128Mx64 Double Data Rate SDRAM high density SODIMM. This dual rank memory module consists of sixteen CMOS 64Mx8 bits with 4 banks Synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin TSSOP package. This module is a 200-pin small-outline dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR SDRAM.

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Two data transfers per clock cycle
- VDD = VDDQ = 2.5V +/-0.2V for DDR333
- JEDEC standard 2.5V I/O (SSTL_2 compatible)
- VDDSPD = 2.3V to 3.6V
- Bi-directional data-strobe (DQS)
- Differential clock inputs (CK and CK#)
- DLL aligns DQ and DQS transition with CK transition
- Programmable read latency: DDR333 (2.5 clock)
- Programmable burst; length (2, 4, 8)
- Programmable burst (sequential & interleave)
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Lead-free, RoHS compliant
- JEDEC pinout
- Gold edge contacts
- PCB: Height 31.75mm (1.250”), double sided component
- Operating temperature (T_A): - Commercial ($0^oC <= T_A <= 70^oC$)
  - Industrial ($-40^oC <= T_A <= +85^oC$)

Pin Description

Pin Name	Function
A0~A12	Row Address Inputs
A0~A9, A11	Column Address Inputs
BA0~BA1	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobes Input/Output
DM0~DM7	Data Mask
CK0, CK0# CK1, CK1#	Clock Input
CKE0, CKE1	Clock Enables Input
CS0#, CS1#	Chip Selects Input
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply
VDDQ	Voltage Supply for DQS
VSS	Ground
VREF	Power Supply Reference
VDDSPD	SPD Voltage Supply
SA1~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
NC	No Connect

Order Information:

VL470L2925 - B3 S G - X

- X — OPERATING TEMPERATURE: None: Commercial; S1: Industrial screening
- G — DRAM DIE: G-DIE
- S — DRAM MANUFACTURER: S - SAMSUNG
- B3 — MODULE SPEED: B3: PC2700 @CL2.5
- VL — VL: Lead-free/RoHS

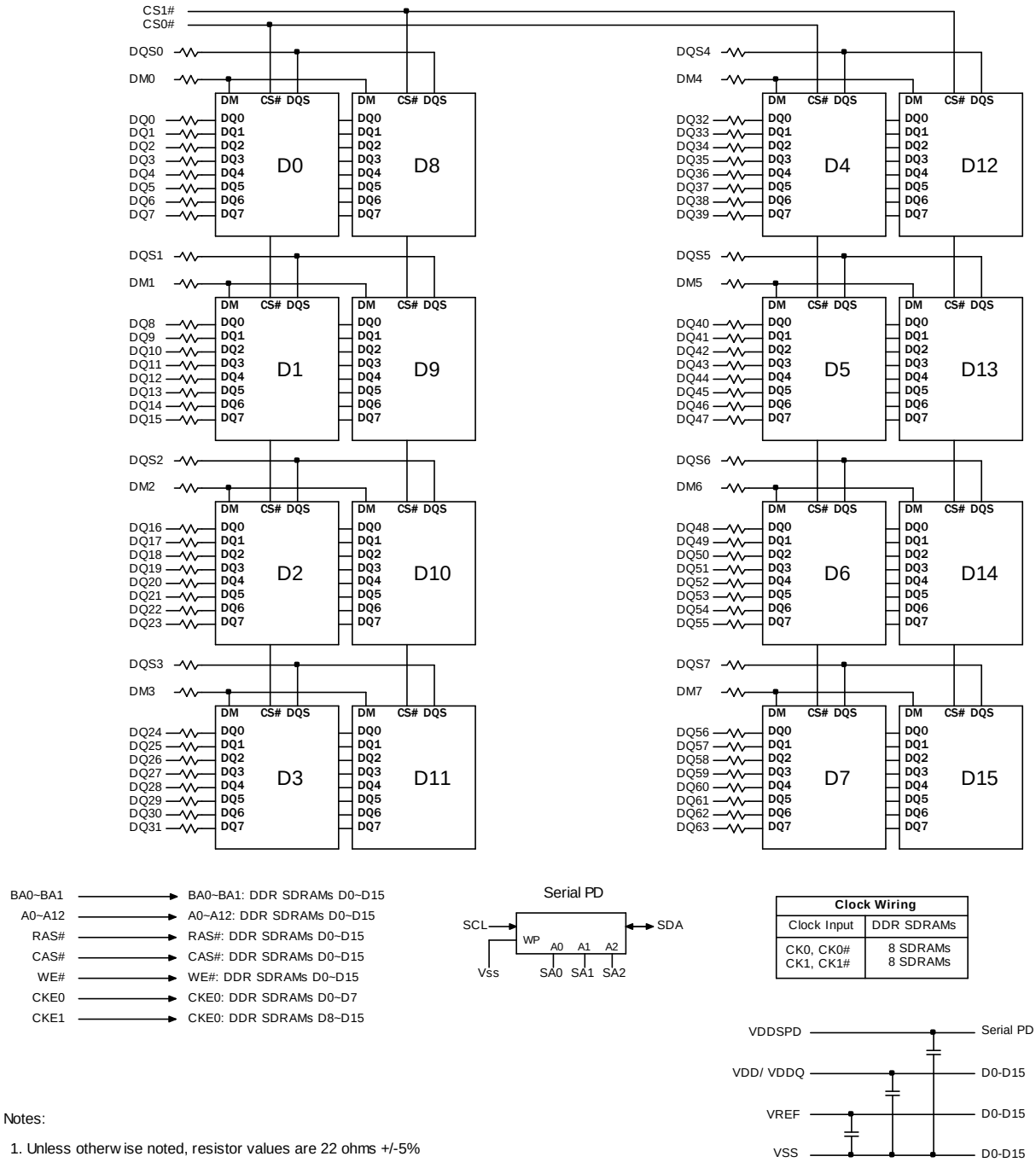
DRAM component: Samsung K4H510838G-HCB3

Pin Configuration

200-PIN DDR SODIMM FRONT								200-PIN DDR SODIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	51	VSS	101	A9	151	DQ42	2	VREF	52	VSS	102	A8	152	DQ46
3	VSS	53	DQ19	103	VSS	153	DQ43	4	VSS	54	DQ23	104	VSS	154	DQ47
5	DQ0	55	DQ24	105	A7	155	VDD	6	DQ4	56	DQ28	106	A6	156	VDD
7	DQ1	57	VDD	107	A5	157	VDD	8	DQ5	58	VDD	108	A4	158	CK1#
9	VDD	59	DQ25	109	A3	159	VSS	10	VDD	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	VSS	12	DM0	62	DM3	112	A0	162	VSS
13	DQ2	63	VSS	113	VDD	163	DQ48	14	DQ6	64	VSS	114	VDD	164	DQ52
15	VSS	65	DQ26	115	A10	165	DQ49	16	VSS	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	VDD	18	DQ7	68	DQ31	118	RAS#	168	VDD
19	DQ8	69	VDD	119	WE#	169	DQS6	20	DQ12	70	VDD	120	CAS#	170	DM6
21	VDD	71	CB0*	121	CS0#	171	DQ50	22	VDD	72	CB4*	122	CS1#	172	DQ54
23	DQ9	73	CB1*	123	NC	173	VSS	24	DQ13	74	CB5*	124	CS2#*	174	VSS
25	DQS1	75	VSS	125	VSS	175	DQ51	26	DM1	76	VSS	126	VSS	176	DQ55
27	VSS	77	DQS8*	127	DQ32	177	DQ56	28	VSS	78	DM8*	128	DQ36	178	DQ60
29	DQ10	79	CB2*	129	DQ33	179	VDD	30	DQ14	80	CB6*	130	DQ37	180	VDD
31	DQ11	81	VDD	131	VDD	181	DQ57	32	DQ15	82	VDD	132	VDD	182	DQ61
33	VDD	83	CB3*	133	DQS4	183	DQS7	34	VDD	84	CB7*	134	DM4	184	DM7
35	CK0	85	CS3#*	135	DQ34	185	VSS	36	VDD	86	NC	136	DQ38	186	VSS
37	CK0#	87	VSS	137	VSS	187	DQ58	38	VSS	88	VSS	138	VSS	188	DQ62
39	VSS	89	CK2*	139	DQ35	189	DQ59	40	VSS	90	VSS	140	DQ39	190	DQ63
41	DQ16	91	CK2#*	141	DQ40	191	VDD	42	DQ20	92	VDD	142	DQ44	192	VDD
43	DQ17	93	VDD	143	VDD	193	SDA	44	DQ21	94	VDD	144	VDD	194	SA0
45	VDD	95	CKE1	145	DQ41	195	SCL	46	VDD	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VDDSPD	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	VSS	199	NC	50	DQ22	100	A11	150	VSS	200	NC

Note: *: These pins are not used in this module.

Function Block Diagram



BA0~BA1 → BA0~BA1: DDR SDRAMs D0~D15
A0~A12 → A0~A12: DDR SDRAMs D0~D15
RAS# → RAS#: DDR SDRAMs D0~D15
CAS# → CAS#: DDR SDRAMs D0~D15
WE# → WE#: DDR SDRAMs D0~D15
CKE0 → CKE0: DDR SDRAMs D0~D7
CKE1 → CKE0: DDR SDRAMs D8~D15

Clock Wiring	
Clock Input	DDR SDRAMs
CK0, CK0# CK1, CK1#	8 SDRAMs 8 SDRAMs

Notes:

1. Unless otherwise noted, resistor values are 22 ohms +/-5%

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
VIN, VOUT	Voltage on any pin relative to VSS		-0.5 ~ 3.6	V
VDD, VDDQ	Voltage on VDD & VDDQ supply relative to VSS		-1.0 ~ 3.6	V
TSTG	Storage temperature		-55 ~ +150	^{0}C
TA	Operating temperature	Commercial	0 ~ 70	^{0}C
		Industrial	-40 ~ +85	
PD	Power dissipation		16	W
IOS	Short circuit current		50	mA

Notes:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

Alls voltages referenced to VSS
TA = 0^{0}C to 70^{0}C

Symbol	Parameter		Min	Max	Unit	Note
VDD	Supply voltage		2.3	2.7	V	
VDDQ	I/O Supply voltage		2.3	2.7	V	
VREF	I/O Reference voltage		0.49 * VDDQ	0.51 * VDDQ	V	1
VTT	I/O Termination voltage		VREF-0.04	VREF+0.04	V	2
VIH(DC)	Input logic high voltage		VREF+0.15	VDDQ+0.30	V	
VIL(DC)	Input logic low voltage		-0.3	VREF-0.15	V	
VIN(DC)	Input voltage level, CK and CK#		-0.3	VDDQ+0.30	V	
VID(DC)	Input differential voltage, CK and CK#		0.3	VDDQ+0.60	V	3
VIX(DC)	Input crossing point voltage, CK and CK#		0.3	VDDQ+0.60	V	
II	Input leakage current	Address, CAS#,RAS#,WE#	-32	32	uA	
		CS#,CKE	-16	16	uA	
		CK, CK#	-16	16	uA	
		DM	-4	4	uA	
IOZ	Output leakage current		-10	10	uA	
IOH	Output high current(normal strength) VOUT = v + 0.84V		-16.8	-	mA	
IOL	Output high current(normal strength) VOUT = VTT - 0.84V		16.8	-	mA	
IOH	Output high current(half strength) VOUT = VTT + 0.45V		-9	-	mA	
IOL	Output high current(half strength) VOUT = VTT - 0.45V		9	-	mA	

Notes:
1. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on VREF may not exceed +/- 2% of the DC value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
3. VID is the magnitude of the difference between the input level on CK and the input level of CK#.

AC Operating Conditions

All voltages referenced to VSS
TA = 0^0C to 70^0C

Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.31	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.31	V
VID(AC)	Input Differential Voltage, CK and CK# inputs	0.70	VDDQ + 0.60	V
VIX(AC)	Input Crossing Point Voltage, CK and CK# inputs	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V

Input/Output Capacitance

TA=25^0C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	CIN1	28	44	pF
Input capacitance (CKE0, CKE1)	CIN2	16	24	pF
Input capacitance (CS0#, CS1#)	CIN3	16	24	pF
Input capacitance (CK0, CK0#, CK1, CK1#)	CIN4	16	24	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	11	13	pF

IDD Specification

Condition	Symbol	B3 (DDR333)	Unit
OPERATING CURRENT: One device bank active; Active-Precharge; tRC=tRC(MIN); tCK=tCK(MIN); DQ,DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	IDD0*	560	mA
OPERATING CURRENT: One device bank; Active-Read-Precharge; BL=4; tRC=tRC(MIN); tCK=tCK(MIN); IOUT =0mA; Address and control inputs change once per clock cycle	IDD1*	680	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks are idle; Power-down mode; tCK=tCK(MIN); CKE=LOW	IDD2P**	80	mA
IDLE STANDBY CURRENT: CS#=HIGH; All device banks are idle; tCK=tCK(MIN); CKE=HIGH; Address and other control inputs changing once per clock cycle. VIN =VREF for DQ,DQS and DM	IDD2F**	368	mA
ACITVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK=tCK(MIN); CKE=LOW	IDD3P**	240	mA
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH; One device bank active; tRC =tRAS(MAX); tCK=tCK(MIN); DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N**	640	mA
OPERATING CURRENT: Burst = 2; Reads; Continnuous burst; One device bank active; Address and other control inputs changing once per clock cycle; tCK=tCK(MIN); IOUT=0mA	IDD4R*	800	mA
OPERATING CURRENT: Burst = 2; Writes; Continnuous burst; One device bank active; Address and other control inputs changing once per clock cycle; tCK=tCK(MIN); DQ, DM and DQS inputs change twice per clock cycle	IDD4W*	840	mA
AUTO REFRESH CURRENT: tRC=tRFC(MIN)	IDD5**	1760	mA
SELF-REFRESH CURRENT: CKE< 0.2V	IDD6**	80	mA
OPERATING CURRENT: Four device bank interleaving Reads Burst=4 with auto precharge; tRC=tRC(MIN); tCK=tCK(MIN); Address and control inputs change only during Active READ, or WRITE commands	IDD7*	1800	mA

Notes:

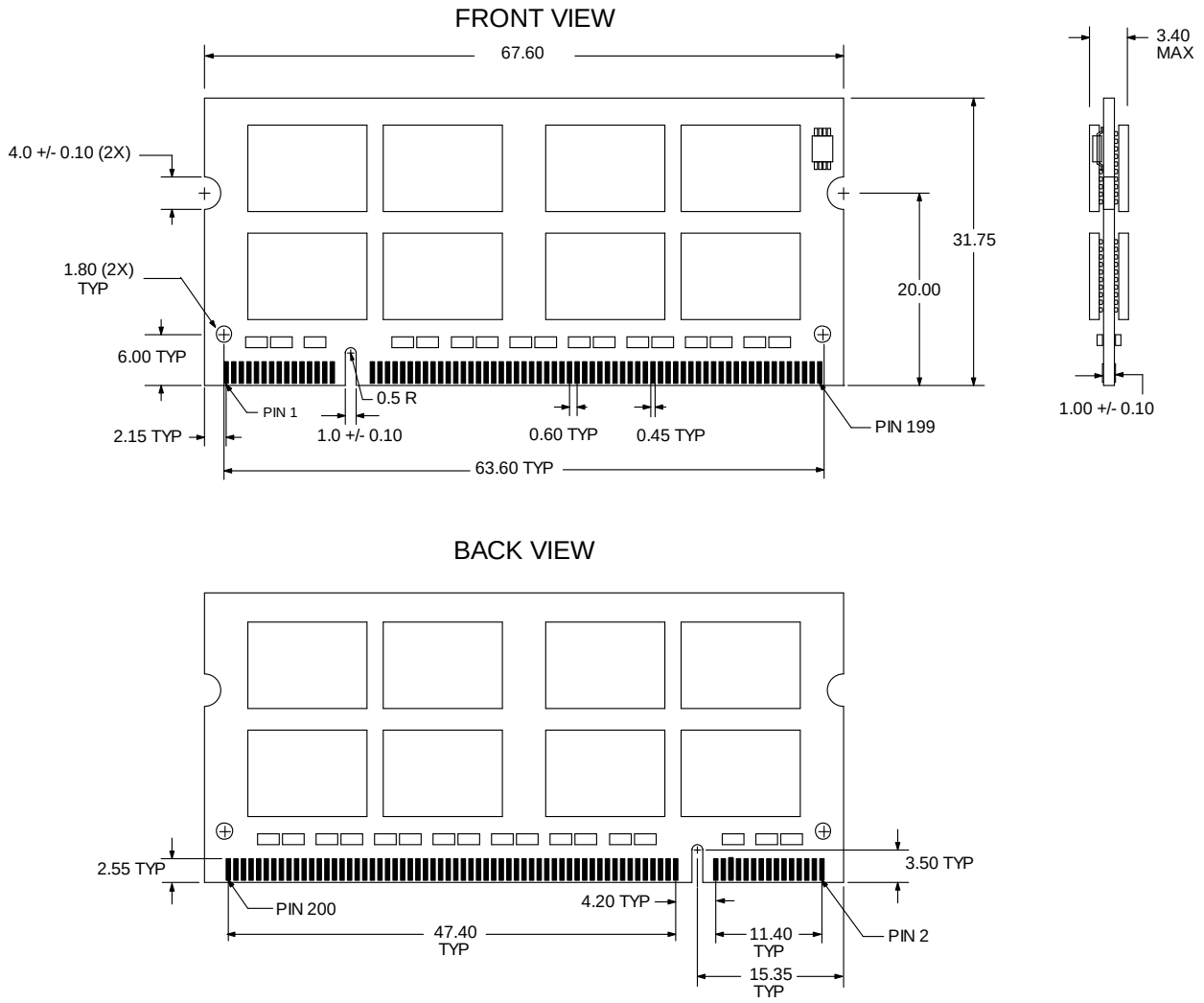
IDD specification is based on Samsung G-die components. Other manufacturers' DRAMs may have different values.

*: Value calculated as one module rank in this operation condition, and other module rank in IDD2P (CKE LOW) mode.
**: Value calculated as all module ranks in this operation condition.

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	CC (DDR400)		B3 (DDR333)		B0 (DDR266)		Unit
			Min	Max	Min	Max	Min	Max	
Row cycle time		tRC	55		60		65		ns
Refresh row cycle time		tRFC	70		72		75		ns
Row active time		tRAS	40	70K	42	70K	45	120K	ns
RAS to CAS delay		tRCD	15		18		20		ns
Row precharge time		tRP	15		18		20		ns
Row active to Row active delay		tRRD	10		12		15		ns
Write recovery time		tWR	15		15		15		ns
Last data in to Read command		tWTR	2		1		1		tCK
Clock cycle time	CL=2.0	tCK	-	-	7.5	12	10	12	ns
	CL=2.5		6	12	6	12	7.5	12	
	CL=3.0		5	10	-	-	-	-	
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS-out access time from CK/CK		tDQSCK	-0.55	+0.55	-0.6	+0.6	-0.75	+0.75	ns
Output data access time from CK/CK		tAC	-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	ns
Data strobe edge to ouput data edge		tDQSQ	-	0.4	-	0.4	-	0.5	ns
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
CK to valid DQS-in		tDQSS	0.72	1.28	0.75	1.25	0.75	1.25	tCK
DQS-in setup time		tWPRES	0		0		0		ns
DQS-in hold time		tWPRE	0.25		0.25		0.25		tCK
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		tCK
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		tCK
DQS-in high level width		tDQSH	0.35		0.35		0.35		tCK
DQS-in low level width		tDQSL	0.35		0.35		0.35		tCK
Address and Control Input setup time(fast)		tIS	0.6		0.75		0.9		ns
Address and Control Input hold time(fast)		tIH	0.6		0.75		0.9		ns
Address and Control Input setup time(slow)		tIS	0.7		0.8		1.0		ns
Address and Control Input hold time(slow)		tIH	0.7		0.8		1.0		ns
Data-out high impedence time from CK/CK		tHZ	-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	ns
Data-out low impedence time from CK/CK		tLZ	-0.65	+0.65	-0.7	+0.7	-0.75	+0.75	ns
Mode register set cycle time		tMRD	10		12		15		ns
DQ & DM setup time to DQS		tDS	0.4		0.45		0.5		ns
DQ & DM hold time to DQS		tDH	0.4		0.45		0.5		ns
Control & Address input pulse width		tIPW	2.2		2.2		2.2		ns
DQ & DM input pulse width		tDIPW	1.75		1.75		1.75		ns
Exit self refresh to non-Read command		tXSNR	75		75		75		ns
Exit self refresh to read command		tXSRD	200		200		200		tCK
Refresh interval time		tREFI		7.8		7.8		7.8	us
Output DQS valid window		tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns
Data hold skew factor		tQHS		0.5		0.55		0.75	ns
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to Read with Auto precharge command		tRAP	15		18		20		
Autoprecharge write recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK
Power Down Exit Time		tPDEX	1		1		1		tCK

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
10/24/2012	1.0	All	Spec release