

ADS5296, 4-Channel 200-MSPS, and 8-Channel 80-MSPS, Analog-to-Digital Converter Evaluation Module

This user's guide gives a general overview of the ADS5296 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the ADS5296 analog-to-digital converters (ADC). The ADS5296 EVM provides a platform for evaluating the ADC under various signal, clock, reference, and ADC output formats.

Contents

1	Quick	View of Evaluation Setup	. 4
2	GUI S	oftware Installation	. 5
	2.1	TSW1400 EVM GUI Installation (High Speed Data Converter Pro (HSDCpro))	. 5
	2.2	ADS5296 EVM GUI Installation	11
3	Hardv	vare and EVM Setup for Testing ADS5296	18
	3.1	External Connections	18
	3.2	ADS5296 EVM Header Configuration	19
	3.3	ADS5296 EVM 0-Ω Jumper Configuration	21
4	Testin	g ADS5296 EVM	24
	4.1	TSW1400 and ADS5296 GUI Setup	24
	4.2	Capturing a RAMP Test Pattern	29
	4.3	Capturing Sinusoidal Input in Octal Non-Interleaving Mode	34
	4.4	Capturing Sinusoidal Input in Quad Interleaving Mode	45
5	ADS5	296 GUI in Detail	50
	5.1	Read Me First Tab	52
	5.2	Top Level Tab	53
	5.3	Test Pattern Tab	57
	5.4	Digital Signal Processing Tab	59
	5.5	Channel Filter Tab	61
6	ADS5	296 EVM Schematics	67
7	ADS5	296 EVM Bill of Materials	76
8	ADS5	296 EVM Layout	78

List of Figures

1	Evaluation Setup	4
2	HSDCpro Install (a)	5
3	HSDCpro Install (b)	6
4	HSDCpro Install (c)	7
5	HSDCpro Install (d)	8
6	HSDCpro Install (e)	9
7	HSDCpro Install (f)	10
8	HSDCpro Install (g)	10
9	HSDCpro Install (h)	11
10	HSDCpro Install (i)	11
11	ADS5296 GUI Install (a)	12
12	ADS5296 GUI Install (b)	13
13	ADS5296 GUI Install (c)	14

ADS5296, 4-Channel 200-MSPS, and 8-Channel 80-MSPS, Analog-to-Digital

1



14/14/14/	ti com	
	паан	

14	ADS5296 GUI Install (d)	15
15	ADS5296 GUI Install (e)	16
16	ADS5296 GUI Install (f)	17
17	ADS5296 GUI Install (g)	18
18	TSW1400 and ADS5296 Setup	19
19	ADS5296 EVM Default Header Configuration	21
20	ADS5296 EVM Octal Non-Interleaving Mode Analog Input SMAs	22
21	ADS5296 EVM Quad Interleaving Mode Analog Input SMAs	23
22	TSW1400 GUI Setup (a)	24
23	TSW1400 GUI Setup (b)	25
24	TSW1400 GUI Setup (c)	25
25	TSW1400 GUI Setup (d)	26
26	TSW1400 GUI Setup (e)	26
27	TSW1400 GUI Setup (f)	26
28	ADS5296 Plug-in GLII Setup (a)	27
29	ADS5296 Plug-in GLII Setup (b)	28
30	ADS5296 Plug.in GUI Setup (c)	20
31	ADS5296 GUI Setup for RAMP Test	30
32	HSDCpro CI II Setup for RAMP Test	31
22		20
24		32
34		33
35		34
36	Jumper J35 and J38 positions for Enabled XTAL (default)	35
37	Jumper J35 and J38 positions for Disabled XTAL	36
38	Octal Non-interleaving Mode Hardware Setup	37
39	ADS5296 GUI Setup for Octal Non-Interleaving Mode	38
40	HSDCpro GUI Setup for Octal Non-Interleaving Mode (b)	39
41	Octal Non-Interleaving Mode Capture 1	40
42	Octal Non-Interleaving Mode Capture 2	41
43	Octal Non-Interleaving Mode Capture 3	42
44	HSDCpro Software Filtering	43
45	HSDCpro Software Filtering Menu	44
46	HSDCpro Capture with Software Filtering	45
47	Quad-Interleaving Mode Hardware Setup	46
48	Quad-Interleaving Mode GUI Setup	47
49	Quad-Interleaving Mode Capture 1	48
50	Quad-Interleaving Mode Capture 2	49
51	Quad-Interleaving Mode Fs/2 - Fin Software Filtering	50
52	ADS5296 GUI Simulation Mode	51
53	ADS5296 GUI Simulation Mode Checkbox Indicator	51
54	RECORD/PLAYBACK COMMAND SEQUENCE (a)	52
55	RECORD/PLAYBACK COMMAND SEQUENCE (b)	53
56	RECORD/PLAYBACK COMMAND SEQUENCE (c)	54
57	DIGITAL WAVEFORM GRAPH-WRITE	54
58	EN SER BIT Drop-Down Menu	55
59	EN SER BIT Info Button	56
60	GENERAL SETUR Section of Top Level Tab	57
61	CLISTOM WRITE/READ Example	57
01		51

www.ti.com		
62	Test Pattern Tab	58
63	PRBS Section Enabled	58
64	TEST PATTERN MODES Section	59
65	Digital Signal Processing Tab	59
66	Digital Signal Processing Tab	60
67	Channel Averaging Info Button	6 0
68	INPUT/OUTPUT MAPPING with EN_INTERLEAVE = 0	61
69	INPUT/OUTPUT MAPPING with EN_INTERLEAVE = 1	61
70	Channel Filter Tab	62
71	EN_DIG_FILTER = 1	63
72	Channel 5 High Pass Filter Enabled	63
73	Channel 1 Digital Filter Enabled	64
74	Channel 1 Pre-Stored Digital Filter Enabled	64
75	Channel 1 Custom Digital Filter Enabled	65
76	Reset Channels on Channel Filter Tab	65
77	Save/Load Custom Filter Coeffs on Channel Filter Tab	66
78	View Filter Coeffs	66
79	ADS5296 Schematic, Sheet 1 of 9	67
80	ADS5296 Schematic, Sheet 2 of 9	68
81	ADS5296 Schematic, Sheet 3 of 9	6 9
82	ADS5296 Schematic, Sheet 4 of 9	70
83	ADS5296 Schematic, Sheet 5 of 9	71
84	ADS5296 Schematic, Sheet 6 of 9	72
85	ADS5296 Schematic, Sheet 7 of 9	73
86	ADS5296 Schematic, Sheet 8 of 9	74
87	ADS5296 Schematic, Sheet 9 of 9	75
88	ADS5296 EVM Top Layer Assembly Drawing – Top View	78
89	ADS5296 EVM Bottom Layer Assembly Drawing – Bottom View	79
90	ADS5296 EVM Top Side	80
91	ADS5296 EVM Ground Plane	81
92	ADS5296 EVM Signal Plane	82
93	ADS5296 EVM Bottom Side	83

List of Tables

1	ADS5296 EVM Header Configuration	20
2	ADS5296 EVM Bill of Materials	76



Quick View of Evaluation Setup

www.ti.com

1 Quick View of Evaluation Setup

Figure 1 is an overview of the evaluation setup that includes the ADS5296 EVM, TSW1400 data capturing card, external equipment, personal computer (PC), and software requirements.



Figure 1. Evaluation Setup

TSW1400 EVM: The high-speed LVDS deserializer board is required for capturing data from the ADS5296 EVM and its analysis using the TSW1400 graphical user interface (GUI), called High Speed Data Converter Pro (*HSDCpro*). For more information pertaining to the TSW1400 EVM, see: http://focus.ti.com/docs/toolsw/folders/print/tsw1400evm.html

Equipment: Signal generators (with low-phase noise) must be used as source of input signal and clock in order to get the desired performance. Additionally, band-pass filters (BPF) are required in signal and clock paths to attenuate the harmonics and noise from the generators. (*Note: Functionality of the setup shown in Figure 1, including the LVDS interface between the ADS5296 and FPGA on the capture card, can be tested using the on-chip test pattern generator and the on-board crystal oscillator for an ADC sampling clock source.*)

Power Supply: A single +5-V supply powers the ADS5296 EVM through connectors located at **J1** and **J2**. The supply for the ADS5296 device is derived from this +5 V supply. The power supply must be able to source up to 1.5 A. The TSW1400 EVM is powered through an AC adaptor provided with its EVM kit.

USB Interface to PC: The USB connections from the ADS5296 EVM and TSW1400 EVM to the personal computer (PC) are used for communication from the GUIs to the boards. Section 2 explains the TSW1400 and ADS5296 GUI installation procedure.

4



2 GUI Software Installation

The ADS5296 EVM and the TSW1400 EVM both require software installations. The following two sections explain where to find and how to install the software properly. Ensure that no USB connections are made to the EVMs until after the installations are complete.

2.1 TSW1400 EVM GUI Installation (High Speed Data Converter Pro (HSDCpro))

From the Texas Instruments website, <u>www.ti.com</u>, search for TSW1400. Under Technical Documents, one will find a **Software** section from which **High Speed Data Converter Pro GUI Installer** can be downloaded and saved (slwc107e.zip or higher).

- Unzip the saved folder and run the installer executable to obtain the menu shown in Figure 2.
- Click the *Install* button.

😻 High Speed Data Converter Pro v2.1 Setup			
Please disconnect any TSW 1400/05/06 boards before installing High Speed Data Converter Pro.			
Installer will now self extract and proceed with installation.			
Cancel Nullsoft Install System v2.46			

Figure 2. HSDCpro Install (a)

• Set the destination directories, or leave as default, for the TSW1400 GUI installation and press the *Next* button as shown in Figure 3.

5



GUI Software Installation

www.ti.com

🕂 🗐 High S	peed Data Converter Pro
	Destination Directory Select the primary installation directory.
	All software will be installed in the following locations. To install software into a different locations, click the Browse button and select another directory.
¢	Directory for High Speed Data Converter Pro C:\Program Files (x86)\Texas Instruments\High Speed Data Converter Pro\ Browse
	Directory for National Instruments products C:\Program Files (x86)\National Instruments\ Browse
	<< Back Next >> Cancel

Figure 3. HSDCpro Install (b)

Read the License Agreement from Texas Instruments and select *I accept the License Agreement* and press the *Next* button as shown in Figure 4. ٠





ų	🖁 High Speed Data Converter Pro			
	License Agreement You must accept the licenses displayed below to proceed.			
	GUI Software Evaluation and Internal Use License Agreement			
	Important - Please read the following license agreement carefully. This is a legally binding agreement. After you read this license agreement, you will be asked whether you accept and agree to the terms of this license agreement. Do not click "I have read and agree" unless: (1) you are authorized to accept and agree to the terms of this license agreement on behalf of yourself and your company; and (2) you intend to enter into and to be bound by the terms of this legally binding agreement on behalf of yourself and your company.			
	 Laccept the License Agreement. I do not accept the License Agreement. 			
	(<u>R</u> ack <u>N</u> ext>> <u>C</u> ancel			

Figure 4. HSDCpro Install (c)

• Read the License Agreement from National Instruments and select *I accept the License Agreement* and press the *Next* button as in Figure 5.

7



GUI Software Installation

www.ti.com

🖳 AD\$5295_96 GUI				
License Agreement You must accept the licenses displayed below to proceed.				
NATIONAL INSTRUMENTS SOFTWARE LICENSE AGREEMENT				
INSTALLATION NOTICE: THIS IS A CONTRACT. BEFORE YOU DOWNLOAD THE SOFTWARE AND/OR COMPLETE THE INSTALLATION PROCESS, CAREFULLY READ THIS AGREEMENT. BY DOWNLOADING THE SOFTWARE AND/OR CLICKING THE APPLICABLE BUTTON TO COMPLETE THE INSTALLATION PROCESS, YOU CONSENT TO THE TERMS OF THIS AGREEMENT AND YOU AGREE TO BE BOUND BY THIS AGREEMENT. IF YOU DO NOT WISH TO BECOME A PARTY TO THIS AGREEMENT AND BE BOUND BY ALL OF ITS TERMS AND CONDITIONS, CLICK THE APPROPRIATE BUTTON TO CANCEL THE INSTALLATION PROCESS, DO NOT INSTALL OR USE THE SOFTWARE, AND RETURN THE SOFTWARE WITHIN THIRTY (30) DAYS OF RECEIPT OF THE SOFTWARE (WITH ALL ACCOMPANYING WRITTEN MATERIALS, ALONG WITH THEIR CONTAINERS) TO THE PLACE YOU OBTAINED THEM. ALL RETURNS SHALL BE SUBJECT TO NI'S THEN CURRENT RETURN POLICY.				
The software to which this National Instruments license applies is ADS5295_96 GUI.				
 I accept the License Agreement. I do not accept the License Agreement. 				
<< Back Next >> Cancel				

Figure 5. HSDCpro Install (d)

• Press the Next button as shown in Figure 6.





ADS5295_96 GUI	
Start Installation Review the following summary before continuing.	
• AD\$5295_96 GUI Files	
Click the Next button to begin installation. Click the Back button to change the installation settings.	
Save File << Back Next >>	Cancel

Figure 6. HSDCpro Install (e)

• The window shown in Figure 7 should appear, indicating that installation is in progress.

9



Igh Speed Data Converter Pro	
Overall Progress: 5% Complete	
-	
	<< Back Next >> Cancel

Figure 7. HSDCpro Install (f)

• The window shown in Figure 8 appears indicating Installation Complete. Press the Next button.

ų	High Speed Data Converter Pro
	Installation Complete
	The installer has finished updating your system.
ŀ	<< Back Next >> Einish

Figure 8. HSDCpro Install (g)

• The window in Figure 9 appears briefly to complete the process.



😻 High Speed D	ata Converter Pro v2.1 Setup: Installing
Execute:	C: \Users \a0193755 \AppData \Local \Temp \HSDCPro \Install \EVM GL
Show details]
Cancel	Nullsoft Install System v2,46 < Back Close

Figure 9. HSDCpro Install (h)

• As shown in Figure 10, a computer restart might be requested depending on whether or not the PC already has the National Instruments' MCR installer. If requested, hit the *Restart* button to complete the installation.



Figure 10. HSDCpro Install (i)

2.2 ADS5296 EVM GUI Installation

Both the ADS5295 and ADS5296 ADCs from Texas Instruments share the same GUI installer. Thus, references to *ADS5295_96* during the installation exist. From the Texas Instruments website, <u>www.ti.com</u>, search for **ADS5296 EVM**. Clicking on the hyperlink in the table will lead to another link titled **ADS5295** and **ADS5296 GUI Installer**, v2.1 (Rev. B). Click on this link to download and save the zipped file (slac547b.zip).

• Unzip the folder and run the Setup.bat file as administrator by right clicking on it and selecting Run as administrator as shown in Figure 11.



w folder					
Name	Da	ate modified	Туре	Size	
🕌 FTDI	5/	13/2013 10:32 AM	File folder		
🐌 Volume	5/	13/2013 10:38 AM	File folder		
README.txt	4/	23/2013 7:28 PM	Text Document		1 K
🚳 Setup.bat		Open	···· - · -··		1 K
		Edit			
		Print			
	()	Run as administra	ator		
		Troubleshoot cor	npatibility		
		7-Zip		+	

Figure 11. ADS5296 GUI Install (a)

• Set the destination directories for the ADS5295_96 GUI installation or leave as default and press the *Next* button as shown in Figure 12.



ADS52	95_96 GUI
	Destination Directory Select the primary installation directory.
	All software will be installed in the following locations. To install software into a different locations, click the Browse button and select another directory.
	Directory for ADS5295_96 GUI C:\Program Files (x86)\Texas Instruments\ADS5295_96\ Browse
	Directory for National Instruments products C:\Program Files (x86)\National Instruments\ Browse
	<< Back Next >> Cancel

Figure 12. ADS5296 GUI Install (b)

• Read the License Agreement from Texas Instruments and select the *I accept the License Agreement* button and then press the *Next* button as shown in Figure 13.



GUI Software Installation

www.ti.com

🛄 ADS5295_96 GUI
License Agreement You must accept the licenses displayed below to proceed.
GUI Software Evaluation and Internal Use License Agreement
Important - Please read the following license agreement carefully. This is a legally binding agreement. After you read this license agreement, you will be asked whether you accept and agree to the terms of this license agreement. Do not click "I have read and agree" unless: (1) you are authorized to accept and agree to the terms of this license agreement on behalf of yourself and your company; and (2) you intend to enter into and to be bound by the terms of this legally binding agreement on behalf of yourself and your company.
 I accept the License Agreement. I do not accept the License Agreement.
<< Back Next >> Cancel

Figure 13. ADS5296 GUI Install (c)

Read the License Agreement from National Instruments and select the I accept the License Agreement ٠ button and then press the Next button as shown in Figure 14.



NATIONAL INSTRUMENTS SOFTWARE LICENSE AGREEMENT
INSTALLATION NOTICE: THIS IS A CONTRACT. BEFORE YOU DOWNLOAD THE SOFTWARE AND/OR COMPLETE THE INSTALLATION PROCESS, CAREFULLY READ THIS AGREEMENT. BY DOWNLOADING THE SOFTWARE AND/OR CLICKING THE APPLICABLE BUTTON TO COMPLETE THE INSTALLATION PROCESS, YOU CONSENT TO THE TERMS OF THIS AGREEMENT AND YOU AGREE TO BE BOUND BY THIS AGREEMENT. IF YOU DO NOT WISH TO BECOME A PARTY TO THIS AGREEMENT AND BE BOUND BY ALL OF ITS TERMS AND CONDITIONS, CLICK THE APPROPRIATE BUTTON TO CANCEL THE INSTALLATION PROCESS, DO NOT INSTALL OR USE THE SOFTWARE, AND RETURN THE SOFTWARE WITHIN THIRTY (30) DAYS OF RECEIPT OF THE SOFTWARE (WITH ALL ACCOMPANYING WRITTEN MATERIALS, ALONG WITH THEIR CONTAINERS) TO THE PLACE YOU OBTAINED THEM. ALL RETURNS SHALL BE SUBJECT TO NI'S THEN CURRENT RETURN POLICY.
The software to which this National Instruments license applies is ADS5295_96 GUI.
 I accept the License Agreement.
I do not accept the License Agreement.
<< Back Next >> Cancel

Figure 14. ADS5296 GUI Install (d)

To begin the installation, press the *Next* button as shown in Figure 15. ٠

Ţexas

www.ti.com

TRUMENTS

ADS5295_96 GUI

License Agreement



GUI Software Installation

www.ti.com

🖳 ADS5295_96 GUI 📃 💻 🖂
Start Installation Review the following summary before continuing.
Adding or Changing • ADS5295_96 GUI Files
Click the Next button to begin installation. Click the Back button to change the installation settings.
Save File << Back Next >> Cancel

Figure 15. ADS5296 GUI Install (e)

• The window shown in Figure 16 should appear showing that installation is in progress.



💭 ADS5295_96 GUI	x
Overall Progress: 25% Complete	
	_
<< Back Next >> Cancel	

Figure 16. ADS5296 GUI Install (f)

• Upon complete of installation, the window in Figure 17 appears. Press the Finish button to continue.



ADS5295_96 GUI		-	
The installer has finished updating your system.			

Figure 17. ADS5296 GUI Install (g)

3 Hardware and EVM Setup for Testing ADS5296

This section outlines the external connections required for ADS5296 EVM as well as the default configuration of the EVM's 3-pin headers and $0-\Omega$ jumper resistors with an explanation of configuration options.

3.1 **External Connections**

The connections shown in Figure 18 should be made for proper hardware setup (Note: Testing the LVDS interface between the ADS5296 EVM and the TSW1400 EVM can be performed using a RAMP function generated within the ADS5296 device in lieu of the signal source listed in item 7 below. Also, an on-board 80-MHz crystal oscillator (XTAL) can provide the ADC sampling clock in lieu of the signal source listed in item 6 below. This configuration is only recommended for testing the RAMP function as low phase noise filtered signal sources must be provided to both the ADC clock input and the ADC analog inputs for measuring device performance).





Figure 18. TSW1400 and ADS5296 Setup

- 1. Mate the TSW1400 EVM at connector **J3** to the ADS5296 EVM at connector **J8** through the high speed ADC interface connector.
- 2. Connect the DC +5-V output of the provided AC-to-DC power supply to **J12 (+5V_IN)** of the TSW1400 EVM and the input of the power supply cable to a 110–230 VAC source.
- 3. Connect +5-V DC power supply leads to connectors J1 (VCC) and J2 (GND) of the ADS5296 EVM.
- 4. Connect the USB cable from PC to J13 (USB) of ADS5296 EVM
- 5. Connect the USB cable from PC to **J5 (USB_IF)** of the TSW1400 EVM. (*Note: it is recommended that the PC USB port be able to support USB2.0. If unsure, always chose the USB ports at the back of the PC chassis over ones located on the front or sides.*)
- Supply an ADC clock signal to SMA J31 (CLK_XFMR) of the ADS5296 EVM (that is, +5 dBm, 80 MHz) but turn off the source as the on board 80-MHz crystal oscillator (XTAL) will be used as a clock source for the initial testing.
- Supply an analog input signal to SMA J15 (CH5_XFMR) of the ADS5296 EVM (that is, +10 dBm, 10 MHz).

3.2 ADS5296 EVM Header Configuration

The ADS5296 EVM is flexible in its configurability through the use of 3 pin headers. The default configuration of the EVM is set to facilitate initial testing requiring minimal bench equipment by providing an 80-MHz ADC sampling clock from an on-board crystal oscillator (XTAL). Table 1 describes the purpose of the 3-pin headers on the EVM while Figure 19 shows the default position. With this configuration, the XTAL, at reference designator **U2**, is powered and providing an 80-MHz signal to a transformer which, in turn, provides a differential sampling clock to the DUT. Table 1 also shows that the default method for selecting even or odd channels in interleaving mode is done through the ADS5296 GUI (**JP14**) as opposed to jumper **JP2** on the EVM.



TEXAS INSTRUMENTS

				icado: comiguia	
Jumper	Default Config	Pin 1 Silkscreen	Pin 3 Silkscreen	Circuit	Description
JP4	short pins 1-2	1.8V_AVDD	+3.3V	Power Supply	Power Supply for DUT: ALWAYS 1.8V_AVDD
J35	short pins 2-3	GND	CDC_3.3V	ADC Sampling Clock	Selects Power supply for CDC chip and on-board XTAL oscillator: (1) GND or (3) +3.3V
J38	short pins 1-2	XTAL	CLK_XFMR	ADC Sampling Clock	Selects ADC sampling clock source: (1) XTAL osc. or (3) external source input to SMA J31 CLK_XFMR
J36	short pins 1-2	XTAL	XTAL_CDC	ADC Sampling Clock	Selects path for XTAL osc. signal: (1) to transformer or (3) to CDC input
J37	short pins 1-2	XTAL	CLK_CDC	ADC Sampling Clock	Selects input source to CDC input: (1) XTAL osc. or (3) external source input to SMA J33 CLK_CDC
J39	short pins 2-3	SE	DIFF	ADC Sampling Clock	Selects ADC sampling clock configuration: (1) Single-ended (3) Differential (must match J40)
J40	short pins 2-3	SE	DIFF	ADC Sampling Clock	Selects ADC sampling clock configuration: (1) Single-ended or (3) Differential (must match J39)
JP2	short pins 1-2	EVEN	ODD	INTERLEAVE_MUX pin	Selects analog input channels to be interleaved: (1) EVEN channels or (3) ODD channels
JP14	short pins 1-2	FTDI	EVM	INTERLEAVE_MUX	Selects source of EVEN/ODD select: (1) GUI control or (3) INTERLEAVE_MUX pin control
JP3	short pins 1-2	1.8V_AVDD	GND	SYNC	SYNC (Note: JP3 and J34 share silkscreen "GND")
J34	short pins 2-3	5V	GND	EXT_REF AMP	Selects Power supply for EXT_REF AMP: (1) +5V or (3) GND (Note: JP3 and J34 share silkscreen "GND")
TP16	short pins 1-2	ADCRESETZ	n/a	SPI	Selects SPI control: (1) GUI control
TP17	short pins 1-2	PD	n/a	SPI	Selects SPI control: (1) GUI control
TP15	short pins 1-2	SDOUT	n/a	SPI	Selects SPI control: (1) GUI control
TP14	short pins 1-2	CSZ	n/a	SPI	Selects SPI control: (1) GUI control
TP12	short pins 1-2	SCLK	n/a	SPI	Selects SPI control: (1) GUI control
TP13	short pins 1-2	SDATA	n/a	SPI	Selects SPI control: (1) GUI control
TP20	short pins 1-2	INTERLEAVE_ MUX	n/a	SPI	Selects SPI control: (1) GUI control

Table 1. ADS5296 EVM Header Configuration





Figure 19. ADS5296 EVM Default Header Configuration

3.3 ADS5296 EVM 0-Ω Jumper Configuration

The ADS5296 can be used an Octal-channel non-interleaving ADC or as a Quad-channel interleaving ADC. The ADS5296 EVM is delivered in a configuration that allows testing both modes without any changes required by the user, except through the software GUI.



Hardware and EVM Setup for Testing ADS5296

www.ti.com

The ADS5296 EVM has eight SMAs vertically mounted on the topside of the board corresponding to eight analog input channels labeled **CHx_XFMR**, where x = 1 to 8, as shown in colored boxes of Figure 20. Channels 5, 6, 7, and 8, highlighted by the yellow box, are configured for octal non-interleaving mode and are driven through the back-to-back transformers on the top side of the board, while channels 1, 2, 3, and 4, highlighted by the blue box, are disconnected from the DUT. This is evident by the installed 0-ohm jumper resistors at **R210**, **R399**, **R209**, **R386**, **R208**, **R394**, **R207**, and **R304** and by the uninstalled 0-ohm resistor jumpers at **R378**, **R379**, **R155**, **R154**, **R166**, **R165**, **R168**, and **R167**, respectively.



Figure 20. ADS5296 EVM Octal Non-Interleaving Mode Analog Input SMAs



The ADS5296 EVM also has four side-mounted SMAs corresponding to four analog input channels labeled CH1_AMP(1,2), CH2_AMP(3,4), CH3_AMP(5,6), CH4_AMP(7,8) as shown in colored boxes of Figure 21. Channels 1 and 2, highlighted by the yellow box, are configured for quad non-interleaving mode and are driven through the amplifiers on the back side of the board, while channels 3 and 4, highlighted by the blue box, are disconnected from the DUT. This is evident by the installed 0-ohm jumper resistors on the backside at **R80**, **R81**, **R324**, and ADS5296, 4-Channel 200-MSPS, and 8-Channel 80-MSPS, Analog-to-Digital Converter Evaluation Module, and by the uninstalled 0-ohm resistor jumpers on the backside at **R346**, **R348**, **R368**, and **R370**, respectively. When an input signal is provided SMA J27, CH1_AMP(1,2), a switch internal to the ADS5296, selects whether ADC channel 1 or ADC channel 2 is sampled. The selection depends on the state of GUI control ODD_EVEN_SEL or on the position of header JP2.



Figure 21. ADS5296 EVM Quad Interleaving Mode Analog Input SMAs



4 Testing ADS5296 EVM

This section outlines the following three test cases with a sub-section dedicated to each case:

- Capturing a RAMP test pattern
- Capturing a Sinusoidal Input in Octal Non-Interleaving Mode
- Capturing a Sinusoidal Input in Quad Interleaving Mode

Only the minimal software GUI settings required to achieve the above tests will be described in this section. For a detailed explanation of the ADS5296 software GUI and all its features, please see Section 5. For a detailed explanation of the *High Speed Data Converter Pro* software GUI, please consult the TSW1400 User's Guide (SLWU079B), available on the Texas Instruments website.

4.1 TSW1400 and ADS5296 GUI Setup

1. With the setup outlined in Figure 18 established, launch the *High Speed Data Converter Pro* GUI. The GUI should automatically detect the serial number of the TSW1400 EVM, connected as shown in Figure 22. Click on *OK*.



Figure 22. TSW1400 GUI Setup (a)

The message shown in Figure 23 will appear. Click OK.





Figure 23. TSW1400 GUI Setup (b)

If instead, the message shown in Figure 24 appears, it indicates that the USB connection to the TSW1400 EVM is not present. Click *OK*, then establish a USB connection and repeat step 1.

49		×
	No Board Connected!	
	ОК	

Figure 24. TSW1400 GUI Setup (c)

2. Select a device by clicking on the Blue arrow in the upper left corner of the *HSDCpro* GUI. Scroll down and select *ADS5296* as shown in Figure 25.



Testing ADS5296 EVM



Figure 25. TSW1400 GUI Setup (d)

Click the Yes button to update the ADC firmware on the TSW1400 FPGA as depicted in Figure 26.



Figure 26. TSW1400 GUI Setup (e)

While the firmware is being loaded into the TSW1400 FPGA, the menu shown in Figure 27 will appear.



Figure 27. TSW1400 GUI Setup (f)

Once loaded, the plug-in ADS5296 GUI will appear as a new tab within the *HSDCpro* GUI as shown in Figure 28.



High Speed Data Converter Pro v2.10

Figure 28. ADS5296 Plug-in GUI Setup (a)

3. Click on the tab *ADS5296 GUI* to view the software GUI for the ADS5296. The GUI consists of two tabs: *Read Me First* and *High Level Test* as shown in Figure 29.

TEXAS INSTRUMENTS

😻 High Speed Data Converter Pro

File Instrument Options Data Capture Options Test Options Device GUI Options Help



Û

- - X



Testing ADS5296 EVM

www.ti.com

File Instru	iment Op	otions Dat	a Capture Options Test Options	Device GUI Options Help				And I av	1		
TE IN	EXAS	MENTS		High Speed	d Dat	a Conver	ter Pro v2.	10			
			ADC		DA	с			ADS5296 GU	I	
AD	DS5296			Read Me First				High Level Test			
Ca	apture							SIMULA	TION		
Test Select	tion							Si	mulation		
Single	e Tone	-						RECOR			
	Value	Unit	1. EVM's DESCRIPTION :	EVM String Description shows the dev	ice conne	ted.			Pecord Sequence		
IR (0.00	dBFs		ADS5296EVM					Record Sequence		
DR	0.00	dBc							Save Sequence		
ID (0.00	dBFs	2. RECORD SEQUENCE :	Allows the user to record sequence du	iring the e	ecution of the cor	mmands.		Diautha du Calaura		
NOB (0.00	Bits	3. SAVE SEQUENCE :	Allows the user to save the recorded s	equence to	o a file			Playback Sequence		
ind. (0.00	dBFs		during the execution of the command	s.			Record	Recorded Sequence Clear Sequence		
orst Spur	0.00	dBFs		Allows the user to playback the saved	-				. Addr	Data	
D2 02	0.00	HZ 0.00E+0	4. PEATDACK SEQUENCE	Allows the user to playback the saved	sequence	in a me.					
D4 (0.00	1.00E+6	5. VERSION INFORMATION :	Version : 2.1 05/10/2013							
D5 (0.00	1.00E+6		Check/Uncheck the radio button pres	ent next t	the drop down					
D6			4. HELP INFO BUTTON	selectors to Open/Close the help and	detailed v	vindow		<	III	- F	
11											
12											
elta Test Parame	eters		OPERATING MODES OF ADS	5296							
Auto Calc	ulation of		Saved Sequence	Mode	n-bit	# of Channels	Fclockmax(MH	z) 1-wire or interleaved	LVDS Data R	ate 🔺	
Coherent F	Frequenci	ies	5296_10b_4ch_even	Even Input Channels Interleaved	10	4	200	Interleaved	1000		
Analysis Win	idow (sam	iples)	5296_10b_4ch_0dd	Non Interleaved	10	4	200	1 wire	1000		
65536	6	•	5296 12b 4ch even	Even Input Channels Interleaved	12	4	160	Interleaved	960	=	
ADC Output	t Data Rat	e	5296 12b 4ch odd	Odd Input Channels Interleaved	12	4	160	Interleaved	960		
ADC Input T) Tarnet Frer		5296_12b_8ch	Non-Interleaved	12	8	80	1-wire	960		
0.0000	00000		5296_14b_8ch_avg_Chx,y	Non-Interleaved, average 2- /4 channels, no decimation	14	8	65	1-wire	910		
			5296_14b_8ch_dec2	Non-Interleaved, decimate by 2	14	8	80	1-wire	560	-	
								Rez	dy	Idle	
		Firmware	Version = "0.2"	TSW 1400 Board	H = TIWA	(A6L		Interface Type = ADC	FIRMWARE		

Figure 29. ADS5296 Plug-in GUI Setup (b)

Clicking on the *High Level Test* tab shows four sub-tabs: *Top Level, Test Pattern, Digital Signal Processing*, and *Channel Filter* as shown in Figure 30.



W High Speed Data Converter Pro File Instrument Options Data Capture Options Test Options											
High Speed Data Converter Pro v2.10											
1000 L			ADC			DAC				ADS5296 GUI	
ADS5296 👽			Read Me First						High Le	vel Test	
	· · · · ·		Top Level	Test Pa	attern	Digital Sig	nal Processing		Channel Filter	SIMULATION	
Tert Cel	capture					origital org	ig			Simulation	
l est Sele	ection			s		GENERAL SETUP			-POWERDOWN MODES -		
sing	pe rone		EN MSB EIDST	LCD Einst						RECORD/PLAYBACK COMMAND SEQUENCE	
C110	Value	Unit		LOD-FIRSt		RST (Soft Reset)	OFF			Record Sequence	
SEDR	0.00	dBrs	BTC_MODE	Offset Binary				·····		Save Sequence	
THD	0.00	dBFs		,		EN_HIGH_ADDR Disab	led Regs ≥ 0x0	8 Addr	PDN_PIN_CFG	Save Sequence	
SINAD	0.00	dBFs	EN_SDR	DDR			Disable 1		PDN_CH1	Playback Sequence	
ENOB	0.00	Bits			_	EN_EXT_REF	Disabled	Ő	PDN_CH2		
Fund. Worst Sper	0.00		FALL_SDR	.CLK Falling Edge			Product.		PDN_CH3	Recorded Sequence	
HD2	dBFs	Hz	EN BIT SER	12-Bite		EN_INTERLEAVE	Disabled	0	PDN_CH4	Index Addr Data 🔺	
HD3	0.00	0.00E+0		12-0105				-	PDN_CH5		
HD4	0.00	1.00E+6	DATA RATE AD	C sampling rate	-	EN_MUX_REG	UD/EVEN SEL by	Pin	PDN_CH6		
HD5	0.00	1.00E+6							PDN_CH7	· · · · · · · · · · · · · · · · · · ·	
1100			PHASE_DDR	10		ODD_EVEN_SEL	ODD	Ö	PDN_CH8	∢	
M1											
M2			DELAY_DATA_R	Tdr = 0ps	•	CUSTOM WRITE/REA	ND	DEVICE PI	N CONTROL	address × 46 Data × 8200	
Delta	neters	<u> </u>		Ten - 150mm		Custom Write Register	·			DIGITAL WAVEFORM GRAPH-WRITE	
Auto Co	loulation of		DELAY_LCLK_R	101 = 199bs		Write Address ×	0		DECET		
Coherent Frequencies			DELAY DATA F	Tdf = 72ps	-	Write Data ×	0		REDEI	SCLK-UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU	
Analysis Window (samples)								INTERLE	AVE_MUX ODD		
655	36	•	DELAY_LCLK_F	Tcf = 120ps	- 0	Write Custom	Register				
ADC Outp	ut Data Ra	te			_	Outer Bred S. 11					
	0					Custom Read Registe	er			<u> </u>	
ADC Input	Target Fre	quency				Read Address ×	0				
0.00	000000					Read Data ×	0				
						record bard					
						Read Custom F	Register			DEVICE STATUS	
										Ready	
										iuic iuic	
			1								
		Firmwar	e Version = "0.2"		T	SW 1400 Board = TIWAKA6L			Interface Ty	Interface Type = ADC_FIRMWARE	
Waiting for	or user in	put		5/	/14/2013 1:3	37:14 PM Build - 04	/30/2013	CONNECTED	Idle	TEXAS INSTRUMENTS	

Figure 30. ADS5296 Plug-in GUI Setup (c)

4. Verify that communication between the ADS5296 EVM and the ADS5296 GUI is established by toggling either PDN_COMPLETE checkbox or the PDN checkbox highlighted on Figure 30. Checking either box should make +5-V power supply current drop from ~850 mA to ~563 mA. If the DC current is approximately 600 mA with both power down boxes unchecked, it indicates that the ADS5296 is not receiving the sampling clock. Please ensure that the 3-pin headers are configured as described in Section 3.2. Before continuing, ensure that both power down boxes are left unchecked. At this point, the GUI is confirmed to be communicating correctly with the EVM and testing can begin.

4.2 Capturing a RAMP Test Pattern

As described in Section 3.1, the LVDS interface between the ADS5296 EVM and the TSW1400 EVM can be tested using the default EVM configuration and minimal bench equipment.

1. Press on the sub-tab labeled *Test Pattern* and select **RAMP PATTERN** within the **TEST_PATT** menu as shown in Figure 31.



Testing ADS5296 EVM

. ---File Instrument Options Data Capture Options Test Options Device GUI Options Help TEXAS INSTRUMENTS High Speed Data Converter Pro v2.10 ADC DAC ADS5296 GUI AD\$5296 • Read Me First High Level Test SIMULATION Test Patterr Digital Signal Processing Channel Filter Top Level Capture Simulation Test Selection Single Tone • RECORD/PLAYBACK COMMAND SEQUENCE Init Record Sequence ۲ PSEUDO-RANDOM BINARY SEQUENCE (PRBS) TEST PATTERN MODES SNR 0.00 dBFs 0.00 dBc dBFs SFDF THD PRBS_TP_EN C Save Sequence TEST PATT -None PRBS_MODE_2 23-bit pattern SINAD 0.00 dBFs ✓ None Playback Sequence ENOB 0.00 RAM PRBS_SEED_FROM_REG Fund. 0.00 dBFs dBFs Clear Sequence DUAL CUSTOM PATTERN Recorded Sequence Wors HD2 HD3 PRBS_SEED 0 🚖 🔘 0.00 SINGLE CUSTOM PATTERN Index Addr Data . dBFs Hz DESKEW PATTERN 0.00F+0 (0x000000 - 0x7EEEE) 0.00 SYNC PATTERN HD4 0.00 1.00E+6 TP_SOFT_SYNC HD5 0.00 1.00E+6 CUSTOM_DATA2 0 HD6 TP_HARD_SYNC • M1 CUSTOM FRAME CLOCK PATTERN -M2 address × F Data × 0 EN_FRAME_PAT Test Parameters M GRAPH Auto Calculation of Coherent Frequencies SCLK- WWWWWWWWWW ADCLKOUT 0 🔄 00-0x3FFF) Analysis Window (samples) SDATA - 0 1 0 65536 • 0 SEN -ADC Output Data Rate 0 ADC Input Target Frequ 0.00000000 DEVICE STATUS Ready Idle Firmware Version = "0.2" TSW 1400 Board = TIWAKA6L Interface Type = ADC_FIRMWARE 5/14/2013 2:15:46 PM Build - 04/30/2013 CONNECTED Idle TEXAS INSTRUMENTS Waiting for user input

Figure 31. ADS5296 GUI Setup for RAMP Test

- 2. Perform the following steps highlighted in Figure 32:
 - (a) Press the ADC tab in HSDCpro
 - (b) Change the plot type from Real FFT to Codes
 - (c) Enter 80M in the field labeled ADC Output Data Rate
 - (d) Press the Capture button





Figure 32. HSDCpro GUI Setup for RAMP Test

3. The saw tooth waveform should be captured and displayed as in Figure 33.



Testing ADS5296 EVM

- - × N High Speed Data Converter Pro . ---File Instrument Options Data Capture Options Test Options Device GUI Options Help TEXAS INSTRUMENTS High Speed Data Converter Pro v2.10 ADC DAC ADS5296 GUI * ADS5296 4095 Codes ,⊕ + Capture Ð 0 Test Selection 10000 20000 55000 5000 15000 25000 30000 35000 40000 45000 50000 60000 65000 70000 0 Time Domain -Codes • Channel 1/8 -Unwrap Waveform Va Unit Overlay 'Unwrap Waveform' Waveform 0.00 Codes 4250 4095.00 ,⊕ + Codes Max St Dev 1182.42 Codes 4000 Ð Mean 2047.50 Codes 3750 Medi 2047 50 Codes RMS Peak to Pe PAR 3500 1182.41 Codes 4095.00 Codes 3250 4.77 dB 3000 2750 2500 Codes Sample 8 2250 M1 2157.00 0.00E+0 M2 2157.00 4.10E+3 2000 P 0.00 4.10E+3 Delt Test Para neters 1750 Auto Calculation of Coherent Frequencies 1500 Analysis Window (samples) 1250 -65536 1000 ADC Output Data Rate 750 80M ADC Input Target Frequ 500 0.00000000 250 1 0ó 5000 10000 15000 20000 25000 30000 35000 40000 45000 50000 55000 60000 65536 Samples ٠ ь Firmware Version = "0.2" TSW 1400 Board = TIWAKA6L Interface Type = ADC_FIRMWARE 5/14/2013 2:29:24 PM Build - 04/30/2013 Waiting for user input Idle TEXAS INSTRUMENTS

Figure 33. RAMP Capture

4. By default, *Channel 1/8* is the first channel displayed. Use the drop-down menu shown in Figure 34 to view all 8 channels and confirm that a saw tooth waveform has been captured. Also confirm, in the menu to the left side, that the min code is 0 and the max code is 4095, corresponding to a 12-bit ADC.





Figure 34. RAMP Capture by Channel

5. Zooming into the waveform, as shown in Figure 35, is recommended to ensure that the RAMP waveform increments 1 ADC code for each subsequent sample.



Testing ADS5296 EVM

www.ti.com



Figure 35. Zoom on RAMP Capture

4.3 Capturing Sinusoidal Input in Octal Non-Interleaving Mode

This section describes the necessary steps to reconfigure the EVM and test setup for capturing a sinusoidal input with the ADS5296 in octal non-interleaving mode.

 The RAMP test described in Section 4.2 was performed using an 80-MHz on-board crystal oscillator (XTAL) for the sampling clock. This clock cannot be used to measure performance of the device as it is not phase locked to the input signal. The XTAL should be disabled by moving jumper J35 from the position labeled CDC_3.3V to the position labeled GND in the silkscreen. Also, J38 must change position from XTAL to CLK_XFMR in the silkscreen to enable the SMA J31 CLK_XFMR. Figure 36 and Figure 37 show the jumper positions before and after this change, respectively.





Figure 36. Jumper J35 and J38 positions for Enabled XTAL (default)



Testing ADS5296 EVM

www.ti.com



Figure 37. Jumper J35 and J38 positions for Disabled XTAL

- 2. With the setup established in Figure 38 and Figure 37, perform the following steps:
 - (a) Enable the signal generator providing the sampling clock to SMA **J31** labeled **CLK_XFMR** (+5 dBm, 80 MHz)
 - (b) Enable the signal generator providing the input signal to SMA J15 labeled CH5_XFMR (+15 dbm, 10 MHz). For high-performance results the instrument should have low phase noise and low harmonic distortion. In addition, a filter is recommended on the input as shown in Figure 38.
 - (c) The two signal generators in items (a) and (b) above should be phase locked so that coherency is established. This is achieved connecting the two via a BNC cable. One instrument will provide 10-MHz output while the other instrument will receive 10-MHz input.




Figure 38. Octal Non-interleaving Mode Hardware Setup

3. Click on *ADS5296 GUI* tab and ensure that the **TEST_PATT** field is set to **None**, as shown in Figure 39.



Testing ADS5296 EVM

Nigh Speed Data Converter Pro - - X Stational Company of Loss . File Instrument Options Data Capture Options Test Options Device GUI Options Help TEXAS INSTRUMENTS High Speed Data Converter Pro v2.10 ADS5296 GUI DAC ADC High Level Test $\mathbf{\Psi}$ ADS5296 Read Me First Test Pattern Top Level Digital Signal Processing Channel Filter Capture Simulation Test Selection -Time Domain PLAYBACK COMMAND SEQUENCE Unit Record Sequence ۲ PSEUDO-RANDOM BINARY SEQUENCE (PRBS) TEST PATTERN MOD 0.00 Codes 4095.00 ۵ Codes PRBS_TP_EN Save Sequence - 0 St De 1182 42 Codes TEST PATT None PRBS_MODE_2 23-bit pattern 2047.50 Codes Playback Sequence Media 2047.50 Codes RAMP_PAT_RESET_VAL 0 * 0 PRBS_SEED_FROM_REG RMS 1182.41 Codes Clear Sequence Peak to F 4095.00 Codes PRBS_SEED 0 🚖 🔘 Add Data PAR 4.77 dB CUSTOM_DATA1 e (0 (0x000000 - 0x7FFFFF) TP_SOFT_SYNC CUSTOM_DATA2 TP_HARD_SYNC -0 Sample (0) 0.00E+0 2157.00 2157.00 4 10F+3 CUSTOM FRAME CLOCK PATTERN Data × address 45 0 4.10E+3 0.00 EN_FRAME_PAT 📃 🔘 Test Para eters Auto Calculation of Coherent Frequencies ADCLKOUT 0 🔄 SCLK-Analysis Window (samples) SDATA - 0 0 65536 -0 SEN -ADC Output Data Rate 80M ADC Input Target Frequ 0.00000000 DEVICE STATUS Idle Firmware Version = "0.2" TSW 1400 Board = TIWAKA6L Interface Type = ADC_FIRMWARE TEXAS INSTRUMENTS Waiting for user input 5/14/2013 3:07:15 PM Build - 04/30/2013 CO Idle

Figure 39. ADS5296 GUI Setup for Octal Non-Interleaving Mode

- 4. Click on the ADC tab and perform the following steps as illustrated in Figure 40.
 - (a) In the box labeled ADC Input Target Frequency input 10M
 - (b) In the drop down menus set Real FFT, Channel 5/8, Rectangular
 - (c) Check the box labeled Auto Calculation of Coherent Frequencies (Note: the ADC Input Target Frequency box will automatically be updated with the required coherent frequency)
 - (d) Change the frequency on the signal generator providing the analog input signal to match the value shown in the ADC Input Target Frequency box (9.99877930 MHz)
 - (e) Press the Capture button





Figure 40. HSDCpro GUI Setup for Octal Non-Interleaving Mode (b)

5. The plot will update as shown in Figure 41. Take note of the *Fund.* value in the left panel highlighted in RED in Figure 41. This value is dependent on the signal level set on the signal generator feeding the input signal to **J15**. It also depends on cable loss and filter insertion loss which can vary among parts. If needed, reset the signal amplitude (level) until the *Fund.* value is approximately –1.0 dBFs, as this is the condition for which the datasheet specifications are set. In the example shown here, the input level should be changed from 15.0 dBm to 15.1 dBm and then a capture retaken.



Testing ADS5296 EVM

💠 High Speed Data Converter Pro File Instrument Options Data Capture Options Test Options Device GUI Options Help TEXAS INSTRUMENTS **High Speed Data Converter Pro** ADC DAC ADS5296 GUI a) 2005 AD\$5296 * 2+ Capture 0 Test Selection 15000 20000 30000 45000 55000 5000 40000 10000 25000 35000 50000 60000 6 65000 70000 Single Tone . Real FFT . . Channel 5/8 Rectangular (Channel 5) 1/1 Averages 0.0 69.67 dEFs 요+ 관 75.06 dBc dBFs -10.0-68.75 dBFs -20.0 -11 M2 -1.09 dBFs -30.0 --88.53 dlic dlic dlic dlic dlic dlic in i -75.06 40.0 -93.73 D4 HD5 -75.06 -50.0 0.00 dBFs Hz -114.82 0.00E+0 -114.66 1.00E+6 -60.0 dB Fs -70.0 eita 0.16 Test Parameters 1.00E+6 -80.0 Auto Calculation of Coherent Frequencies -90.0 Analysis Window (sample 65536 -100.0 ADC Sampling Rate (Fs) -110.0 80M ADC Input Target Frequer -120.0 9,99877930M -130.0 2M 4M 6M 10M 12M 14M 16M 18M 20M 22M 24M 26M 28M 30M 32M 34M 36M 38M 40M 8M ö Frequency (Hz) ۰. . Firmware Version = "0.0" TSW 1400 Board = TIVNUM09 Interface Type = ADC_FIRMWARE TEXAS INSTRUMENTS 2/24/2013 9:53:37 PM Build - 01/29/2013 Idle Waiting for user input

Figure 41. Octal Non-Interleaving Mode Capture 1

6. After re-capturing, the Fund. value is now closer to -1.0 dBFs as shown in Figure 42.





Figure 42. Octal Non-Interleaving Mode Capture 2

The SNR computed is highly dependent on the phase noise of the input signal source. Figure 42 and Figure 43 are with the exact same configuration, the only difference being the instrument used to provide the 10-MHz input signal. A 4.5 dB difference in the computed SNR is observed and is attributed solely to the integrity of the input signal, specifically the close-in phase noise.



Testing ADS5296 EVM

- -+ High Speed Data Converter Pro - - X Device GUI Options Help File Instr nent Options Data Capture Options Test Options TEXAS INSTRUMENTS High Speed Data Converter Pro v2.10 . ADC DAC ADS5296 GUI AD55296 4095 Codes 2+ Capture ð 0 Test Selection 10000 50000 55000 5000 15000 20000 25000 30000 35000 40000 45000 60000 65000 70000 • Single Tone Rectangular 💌 1/1 Averages Real FFT . Channel 5/8 (Channel 5) 10.0 65.23 74.93 72.76 d8/1 <u>8</u>+ dik dilfs 0.0 1 72.76 64.85 10.48 -0.58 -84.68 -87.81 d87s 8its d87s d87s d86 d8c d8c d8c d8c d8c d8c 100 100 100 100 100 100 100 -10.0--20.0 --30.0 --34,93 -34,93 -34,20 -34,93 -40.0 6.00 -50.0 -110.38 dBFi -60.0 -116.90 6.51 1.006+6 -70.0 Test Par eters -80.0 Auto Calculation of Coherent Frequenci -90.0 Analysis W ndow (sample 65536 Rate -100.0 --110.0 -80M ADC Input Target Freq -120.0 9.99877930M -130.0 24M 26M 28M 6M 8M 18M 20M 22M 30M 32M 34M 36M ó 2М 414 10M 12M 14M 16M 38M Frequency (Hz) ۰. Firmware Version - "0.2" TSW 1400 Board - TIWAKA6L Interface Type = ADC_FIRMWARE TEXAS INSTRUMENTS 5/8/2013 9:03:56 AM Build - 04/30/2013 Waiting for user input Idle

Figure 43. Octal Non-Interleaving Mode Capture 3

A software filter can be used to remove the contribution of phase noise using the *HSDCpro* menu *Test Options* => *Frequency Bins* as shown in Figure 44.





Figure 44. HSDCpro Software Filtering

Change the default values from 0 to 500 as shown in Figure 45.



V Filter Parameters		x						
Filter Parameters								
Number of bins to remove on eith	er side of fundamental							
500								
Number of bins to remove on eith	er side of harmonics							
500								
Number of bins to remove after D	с							
25								
Number of Harmonics								
5								
Frequency notch parameters								
Frequency Number of bins to remove on either side								
30.0012M	0	*						
0	0							
0	0	Ŧ						
To delete a particular frequency, ple frequency and choose "Delete Elem Frequency Notching Example: For interleaved spur, fs/2 - fin = 30.001221M	ease right click on the ent".							

Figure 45. HSDCpro Software Filtering Menu

The plot and all calculations will be updated accounting for these removed bins as shown in Figure 46. The SNR is now very close to the Software Filtering Menu SNR shown in Figure 43 using a superior instrument.





Figure 46. HSDCpro Capture with Software Filtering

4.4 Capturing Sinusoidal Input in Quad Interleaving Mode

This section describes the necessary steps to reconfigure the EVM and test setup for capturing a sinusoidal input with the ADS5296 in quad interleaving mode.

- 1. Setup the EVM as shown in Figure 47 by performing the following steps:
 - (a) The signal generator providing the sampling clock to SMA **J31** labeled **CLK_XFMR** should be changed from 80 MHz to 200 MHz. (+5 dBm, 200 MHz)
 - (b) Provide the input signal to SMA **J27** labeled **CH1_AMP(1,2)** (+15.1 dbm, 10 MHz). For highperformance results the instrument should have low phase noise and low harmonic distortion. In addition, a filter is recommended on the input as shown in Figure 47.
 - (c) The two signal generators in items (a) and (b) above should be phase locked. This is achieved connecting the two via a BNC cable. One instrument will provide 10-MHz output while the other instrument will receive 10-MHz input.



Testing ADS5296 EVM



Figure 47. Quad-Interleaving Mode Hardware Setup

- 2. From the ADS5296 GUI, Top Level tab, make the following changes as shown in Figure 48. With this configuration the ADS5296 will be sampling channel 1 since the ODD EVEN SEL is set to ODD in the software GUI.
 - (a) Change EN_BIT_SER to 10-bits
 - (b) Change EN_INTERLEAVE to Enabled
 - (c) Change ADC Output Data Rate to 200M
 - (d) Reset the signal generator providing the analog input signal to the new coherent frequency shown in the ADC Input Target Frequency box (9.98229980 MHz)
 - (e) Return to ADC tab and hit Capture.



No. High Speed Data Convert	ter Pro		and the second second	
File Instrument Options	Data Capture Options Test Options Device	e GUI Options Help		
TEXAS INSTRUMENTS		High Speed Data Conv	verter Pro v2.10	
1 1	ADC	DAC		ADS5296 GUI
ADS5296	Rea	d Me First	High Le	vel Test
Canture	Top Level Tes	st Pattern Digital Signal Processing	Channel Filter	SIMULATION
Test Selection				Simulation
Single Tone 💌	OUTPUT INTERFACE MODES	GENERAL SETUP	POWERDOWN MODES	RECORD/PLAYBACK COMMAND SEQUENCE
Value Unit	EN_MSB_FIRST LSB-First	RST (Soft Reset)	PDN PARTIAL	Perord Sequence
SNR 61.30 dBFs			PDN_COMPLETE	Record Sequence
SFDR 69.95 dBc	BTC_MODE Offset Binary	EN_HIGH_ADDR Disabled Regs ≥ 0x0	C8 Addr PDN_PIN_CFG	Save Sequence
THD 68.79 dBFs	EN SDR DDR		PDN_CH1	Disubards Camunate
ENOB 9.83 Bits		EN_EXT_REF Disabled	PDN_CH2	
Fund2.03 dBFs	FALL_SDR LCLK Falling Edg	ge	PDN_CH3	Recorded Sequence Clear Sequence
HD2 -80.90 dBr		EN_INTERLEAVE Enabled	PDN_CH4	Index Addr Data 🔺
HD3 -69.95 dBc	EN_BIT_SER 10-Bits		PDN_CH5	
HD4 -91.08 dBc	DATA_RATE ADC sampling rate	e 🗸 💿 EN_MUX_REG ODD/EVEN SEL by	PDN_CH6	
HD5 -69.95 dBc			PDN_CH7	
dBFs Hz	PHASE_DDR 10	ODD_EVEN_SEL ODD	PDN_CH8	4
M1 -106.46 0.00E+0				
Delta 4.71 1.00E+6	DELAT_DATA_R	CUSTOM WRITE/READ	DEVICE PIN CONTROL	address × 55 Data × 0
Test Parameters	DELAY_LCLK_R Tcr = 159ps	Write Address X 0	PDN	DIGITAL WAVEFORM GRAPH-WRITE
Auto Calculation of		White Address	RESET	SCLK-70000000000000000000000000000
Coherent Frequencies Analysis Window (samples)	DELAY_DATA_F Tdf = 72ps	Vrite Data × 0		
65536	DELAY LCLK F Tcf = 120ps	Write Custom Register	INTERLEAVE_MOX ODD	
ADC Output Data Rate				SEN - 0
200M <	3	Custom Read Register		
ADC Input Target Frequency		Read Address × 0		
9.98229980M	3	Read Data × 0		
		Read Custom Register		DEVICE STATUS
				Ready Idle
Firmwa	are Version = "0.2"	TSW 1400 Board = TIWAKA6L	Interface T	ype = ADC_FIRMWARE
Waiting for user input		5/14/2013 5:00:53 PM Build - 04/30/2013	CONNECTED Idle	TEXAS INSTRUMENTS

Figure 48. Quad-Interleaving Mode GUI Setup

Figure 49 shows that the Fund. value is ~0.8 dB low.



Testing ADS5296 EVM



Figure 49. Quad-Interleaving Mode Capture 1

Increasing the output power from the signal generator by +0.8 dB and re-capturing results in Figure 50.

						ц 🖤						
DS5296		ຢ 1023 -										
Capture		3										
ection		ľ č	5000	10000	15000	20000	25000	30000	35000	40000	45000	50000
le Tone	-		Real FFT	-	Channel 1	/4 💌	Recta	ngular 💌	(Char	nnel 1)		1/1 A
Value	Unit	10.0							-			
60.62	dBFs	10.0-										
72.96	dBc	0.0-										
78.20	dBFs	0.0-		- 1								
60.54	dBFs	10.0-										
9.76	Bits	-10.0										
-1.01	dBFs	-20.0-14	2									
-73.98	dBFs 🗲		-									

See Sec. and

File Instrument Options Data Capture Options Test Options Device GUI Options Help

ADC

-30.0

-40.0

-50.0

-60.0

-70.0

-80.0

-90.0

-100.0

-110.0

-120.0

-130.0-

.€

Firmware Version = "0.2"

ó 5M

R E E

Figure 50. Quad-Interleaving Mode Capture 2

35M

TSW 1400 Board = TIWAKA6L

5/14/2013 5:35:40 PM Build - 04/30/2013

10M 15M 20M 25M 30M

For an interleaving ADC, there exists a spur at Fs/2-Fin, which is commonly referred to as the interleaving spur. As seen in the previous capture, this spur is the Worst Spur in the Nyquist band. The HSDCpro GUI auto-calculates the location of this spur in the menu Test Options \rightarrow Notch Frequency Bins and allows for removal this bin from the plot if desired as shown in Figure 51.

Frequency (Hz)

High Speed Data Converter Pro v2.10

DAC



ADS5296 GUI

65000

90M

Interface Type = ADC_FIRMWARE

Idle

95M 100M

TEXAS INSTRUMENTS

60000

55000

Averages

ANY YANYA MAYARA MANA

40M 45M 50M 55M 60M 65M 70M 75M 80M 85M

- - X

,⊕ + ŝ,

,⊕ +

9

70000



🟘 High Speed Data Converter Pro

TEXAS INSTRUMENTS

dBFs dBc dBc dBc dBc dBc dBc dBc Hz 0.00E+0

1.00E+6

1.00E+6

-

-78.66

-84.16 -92.85

-89.39

0.00

dBFs

2.54

eters

Auto Calculation of Coherent Frequencies

Analysis Window (samples) 65536

ADC Output Data Rate

200M ADC Input Target Frequ

9.98229980M

Waiting for user input

-105.77

-108.30

=

Test Sel

SEDE

INAL NOB nd orst St

D2

HD3

D5

ID6

M1

Test Para

Sind



ADS5296 GUI in Detail

www.ti.com

	Filter Parameters	5					
	Number of bins to	o remove on e	either side of fundamental				
	0						
	Number of bins to	remove on e	either side of harmonics				
	0						
	Number of bins to	o remove afte	r DC				
	1						
	Number of Harmo	onics					
	5						
	Frequency		Number of bins to remove on either side	2			
-	90.0	0177M	0	1			
		0	0				
		0	0				
	To delete a particular frequency, please right click on the						
	frequency and cho	ose "Delete El	lement".				
	Frequency Notchin For interleave	ng Example: ed spur,	or or				

Figure 51. Quad-Interleaving Mode Fs/2 - Fin Software Filtering

5 ADS5296 GUI in Detail

This section is dedicated to explaining the ADS5296 GUI, and all its features, in depth. There is a section dedicated to each tab of the ADS5296 software GUI: *Read Me First, Top Level, Test Pattern, Digital Signal Processing*, and *Channel Filter*.

After launching *HSDCpro*, the ADS5296 GUI can be invoked in two ways: normal mode or simulation mode. Simulation mode is used in the event that no ADS5296 EVM is available. When this is the case, the message shown in Figure 52 appears shortly after choosing the ADS5296 device in *HSDCpro*.





Figure 52. ADS5296 GUI Simulation Mode

The user is given the choice to *Continue in Simulation* or *Stop & Close*. If *Continue in Simulation* is selected the ADS5296 GUI will install and all controls will "*appear*" to function as normal including the *DIGITAL WAVEFORM GRAPH-WRITE* which shows what is being written to the serial interface. When in *Simulation* mode the checkbox at the top right corner of the GUI will remain checked as shown in Figure 53.

High Speed D	ata Converter	Pro							
e Instrument	Options Da	ta Capture Options Test Options	Device GUI Options Help						
TEXAS INSTR	UMENTS		High Speed	l Dat	a Convert	er Pro v2.10			
	,	ADC		DA	c		Α	DS5296 GUI	
ADS529	6 🔽		Read Me First				High Level Test		
Cantur							SIMULATI	ON	
Test Selection							🗾 📝 Simu	lation	
Single Ton	-						PECOPD /		
ungre ron			D/M Chine Description shows the des				RECORD		
Value	Unit	1. EVMIS DESCRIPTION :	Evivi String Description shows the dev	ice conne	cted.		R	ecord Sequence	
R 0.00	dBc		ADS5296EVM					Save Sequence	
0.00	dBFs	2. RECORD SEQUENCE :	Allows the user to record sequence du	iring the e	execution of the com	mands.			
D 0.00	dBFs						Pla	ayback Sequence	
3 0.00	Bits	3. SAVE SEQUENCE :	Allows the user to save the recorded s	equence t	to a file			Cle	ar Sequence
t Spur 0.00	dBFs		during the execution of the command	5.			Recorded	Sequence	
dBFs	Hz	4. PLAYBACK SEQUENCE :	Allows the user to playback the saved	sequence	e in a file.		Index	Addr	Data
0.00	0.00E+0		Version + 2 1 05/10/2012						
0.00	1.00E+6	5. VERSION INFORMATION :	Version: 2.1 05/10/2015						
0.00	1.00040	4. HELP INFO BUTTON 🔘 :	Check/Uncheck the radio button pres	ent next t	to the drop down		4		
			selectors to Open/Close the help and	detailed	window				
a		OPERATING MODES OF ADS	5206						
t Parameters		Saved Sequence	Mode	n.hit	# of Channels	Eclockmax(MHz)	1.wire or interleaved	LVDS Data Pat	
uto Calculatio	n of	5296 10b 4ch even	Even Input Channels Interleaved	10	4	200	Interleaved	1000	- A
oherent Frequ	encies	5296 10b 4ch odd	Odd Input Channels Interleaved	10	4	200	Interleaved	1000	
CEEDC	samples)	5296 10b 8ch	Non-Interleaved	10	8	100	1-wire	1000	
00000 C Output Date	Rate	5296_12b_4ch_even	Even Input Channels Interleaved	12	4	160	Interleaved	960	=
0	- Sale	5296_12b_4ch_odd	Odd Input Channels Interleaved	12	4	160	Interleaved	960	
C Input Tarnet	Frequency	5296_12b_8ch	Non-Interleaved	12	8	80	1-wire	960	
0.00000000 5296_14b_8ch_avg_Chx,y			Non-Interleaved, average 2- /4 channels, no decimation	14	8	65	1-wire	910	
		5296_14b_8ch_dec2	Non-Interleaved, decimate by 2	14	8	80	1-wire	560	-
							Ready	(I	dle
	Firmware	Version = "0.2"	TSW 1400 Board	H = TIWA	KA6L		Interface Type = ADC F	IRMWARE	

Figure 53. ADS5296 GUI Simulation Mode Checkbox Indicator

As Figure 53 shows, within the ADS5296 GUI tab there are two high level tabs called *Read Me First* and *High Level Test*. The *Read Me First* tab contains general information while the *High Level Test* tab holds four sub-tabs containing all SPI controls.



5.1 Read Me First Tab

After launching *HSDCpro* and selecting the ADS5296 firmware to load, as depicted in Figure 22 through Figure 27, the ADS5296 GUI presents the *Read Me First* tab initially as shown in Figure 53 (*Simulation* checkbox will be unchecked if EVM is connected).

The two sections in the upper right corner of this tab, *SIMULATION* and *RECORD/PLAYBACK COMMAND* SEQUENCE, are common to all tabs within the ADS5296 GUI. The *RECORD/PLAYBACK COMMAND* SEQUENCE section allows the user to:

- Record a sequence of commands
- Save the sequence that was recorded to a file
- Playback a sequence that was saved from a file

Once the *Record Sequence* button is pressed, the sequence of commands, or SPI writes, will appear chronologically in the Recorded Sequence box at the bottom of this section as depicted in Figure 54.

RECORD/PLAYBACK COMMAND SEQUENCE							
Record Sequence							
Save Sequence							
Playback Sequence							
Recorded Sequence							
Index	Addr	Data					
0	7	3					
1	50	0					
0	7	2	-				
•	III		•				

Figure 54. RECORD/PLAYBACK COMMAND SEQUENCE (a)

Hitting the Save Sequence button brings up dialog box to save the sequence to the GUI install path:

C:\Program Files (x86)\Texas Instruments\ADS5295_96\Recorded Sequences\ADS5296 Recorded Sequences

To playback a saved sequence, hit the *Playback Sequence* button and choose the sequence to execute. As shown in Figure 55, there are nine sequences pre-defined in this folder corresponding to the nine *OPERATING MODES OF ADS5296* shown in the table at the bottom of the tab. The table includes the maximum sampling clock speed supported for each mode. Ensure that the clock source is within this limit for a particular mode.





Noose or Ente	er Path of File	_	X
Save in:	DS5296 Recorded Sequences	G 🤌 📂 🖽 -	
Æ	Name	Date modified	Туре
2	5296_10b_4ch_even.ini	2/22/2013 7:20 AM	Configura
Recent Places	5296_10b_4ch_odd.ini	2/22/2013 7:20 AM	Configura
	5296_10b_8ch.ini	2/22/2013 7:20 AM	Configura
	5296_12b_4ch_even.ini	2/22/2013 7:20 AM	Configura
Desktop	15296_12b_4ch_odd.ini	2/22/2013 7:20 AM	Configura
	125296_12b_8ch.ini	2/22/2013 7:20 AM	Configura
	5296_14b_8ch_avg_ch1,2.ini	2/22/2013 7:20 AM	Configura
Libraries	5296_14b_8ch_dec2.ini	2/22/2013 7:20 AM	Configura
	الله 5296_16b_8ch_dec8.ini	2/22/2013 7:20 AM	Configura
Computer			
Naturali	•		Þ
INELWOIK	File name:	-	ОК
	Save as type: Custom Pattern (*.ini;*.bd)	•	Cancel

Figure 55. RECORD/PLAYBACK COMMAND SEQUENCE (b)

5.2 Top Level Tab

The left-most sub-tab within the *High Level Test* tab is *Top Level*. As shown in Figure 56, this tab contains five sections which are highlighted in red: *OUTPUT INTERFACE MODES*, *GENERAL SETUP*, *POWERDOWN MODES*, *CUSTOM WRITE/READ* and *DEVICE PIN CONTROL*. In the right border of this tab is a section called *DIGITAL WAVEFORM GRAPH-WRITE*.



ADS5296 GUI in Detail

😻 High Sp	eed Data	Converter	r Pro			-				
File Insti	TEXAS	MENTS	ata Capture Options Test C	Options Device	Hig	⊣ep Ih Speed Da	ata Conve	erter Pro	O v2.10	
,			ADC				DAC			ADS5296 GUI
	ADS5296	V		Rea	d Me First				High Le	vel Test
	Canture		Top Level	Tes	st Pattern	Digital	Signal Processing		Channel Filter	SIMULATION
Test Sel	ection						-			Simulation
Sing	le Tone	-		DDES		- GENERAL SETUP -			-POWERDOWN MODES -	RECORD/PLAYBACK COMMAND SEQUENCE
	Value	Unit	EN_MSB_FIRST	LSB-First		RST (Soft Reset)	OFF		PDN_PARTIAL	Record Sequence
SNR	0.00	dBFs	BTC MODE	011 10					PDN_COMPLETE	
SFDR	0.00	dBc	BIC_MODE	Offset Binary		EN_HIGH_ADDR Dis	abled Regs ≥0xC8	Addr	PDN_PIN_CFG	Save Sequence
SINAD	0.00	dBFs	EN_SDR	DDR					PDN_CH1	Playback Sequence
ENOB	0.00	Bits				EN_EXT_REF	Disabled	0	PDN_CH2	
Fund. Worst Spur	0.00	dBFs dBFs	FALL_SDR	LCLK Falling Edg	ge		Disabled		PDN_CH3	Recorded Sequence
HD2	dBFs	Hz	EN_BIT_SER	12-Bits		EN_INTERLEAVE	Disabled		PDN_CH4	Index Addr Data 🔺
HD3	0.00	0.00E+0				EN MUX PEG	ODD/EVEN SEL by Pi	in O	PDN_CH5	
HD4 HD5	0.00	1.00E+6	DATA_RATE	ADC sampling rate	e 🔽 🔘		,		PDN_CH6	
HD6				10		ODD_EVEN_SEL	ODD	0	PDN_CH2	4 III >
M1			FINAL_DOK	10					PDIV_CITIS	
M2			DELAY_DATA_R	Tdr = 0ps	•	-CUSTOM WRITE/R	EAD -	DEVICE PI	N CONTROL -	address × 55 Data × 0
Delta Test Parar	neters			Ter - 000		Custom write Regi	ster		PDN I	DIGITAL WAVEFORM GRAPH-WRITE
Auto Ca	loulation o	f	DELAT_LOLK_R	Ter = ops		Write Address ×	0		RESET	
Coheren Analysis W	it Frequen indow (sar	cies nples)	DELAY_DATA_F	Tdf = 0ps	•	Write Data ×	0	INTERI E		
655	36	•	DELAY_LCLK_F	Tcf = 0ps	•	Write Cust	om Register			SEN-] 0 [
ADC 0010	0M					Custom Read Reg	ister			
ADC Input	Target Fre	quency				Read Address ×	0			
15.506	559180M					Dead Data in	0			
						Kead Data ×	0			
						Read Custo	m Register			DEVICE STATUS
										Ready Idle
		Firmwar	e Version = "0.2"		1	TSW 1400 Board = TIV	/AKA6L		Interface Ty	/pe = ADC_FIRMWARE
Waiting f	or user in	put			5/16/2013 6:	:57:04 PM Build - (04/30/2013	CONNECTED	Idle	TEXAS INSTRUMENTS

Figure 56. RECORD/PLAYBACK COMMAND SEQUENCE (c)

This section, like *Simulation* and *RECORD/PLAYBACK COMMAND SEQUENCE* above it, remains fixed in the border when switching among the sub-tabs within the *High Level Test* tab. The *DIGITAL WAVEFORM GRAPH-WRITE* section, shown in Figure 57, tracks all SPI writes from the GUI and displays them here.

address × 42	Data × 8000
DIGITAL WAVEFOR	RM GRAPH-WRITE
SCLK - UNI SDATA - 0 SEN -	₩₩₩₩₩₩₩₩₩₩₩₩ 0

Figure 57. DIGITAL WAVEFORM GRAPH-WRITE

The OUTPUT INTERFACE MODES section contains all device controls related to the format of the data to be output across the LVDS interface. Figure 58 shows the drop-down menu for **EN_SER_BIT** which selects the resolution of he ADC. The button to the right of this menu, and seen throughout the GUI, is an info button and displays relevant information from the datasheet.



www.ti.com	www.ti.	com
------------	---------	-----

-OUTPUT INTERFACE	MODES	
EN_MSB_FIRST	LSB-First	
BTC_MODE	Offset Binary	
EN_SDR	DDR	
FALL_SDR	LCLK Falling Edge	
EN_BIT_SER	12-Bits 💌	\bigcirc
DATA_RATE	10-Bits ✓ 12-Bits	\circ
PHASE_DDR	14-Bits 16-Bits	0
DELAY_DATA_R	Tdr = 0ps	0
DELAY_LCLK_R	Tcr = 0ps	\bigcirc
DELAY_DATA_F	Tdf = 0ps ▼	\bigcirc
DELAY_LCLK_F	Tcf = 0ps	\bigcirc

Figure 58. EN_SER_BIT Drop-Down Menu

When the info button next the **EN_SER_BIT** control is selected with **12-bits** selected the information shown in Figure 59 is presented.



ADS5296 GUI in Detail

www.ti.com





The *GENERAL SETUP* section shown in Figure 60 contains several controls, the top most being the **RST** button, or software reset. When this button is pressed all serial registers are updated to their default state and the bit is reset automatically. The button **EN_HIGH_ADDR** is required to enable the **EN_EXT_REF** button below it. This dependency represents the implementation in the design itself. The ADS5296 device supports both internal and external reference mode to set the full-scale of the ADC. The **EN_INTERLEAVE** button is used to enable and disable the interleaving mode, thus, switching the device between a quad channel ADC and an octal ADC, respectively. When **EN_INTERLEAVE** is enabled, the **EN_MUX_REG** button becomes active (ungreyed) and determines whether the selection to sample odd numbered channels or even numbered channels in interleave mode comes from the SPI or from the **INTERLEAVE_MUX** pin of the device. If *ODD/EVEN SEL* by SPI is selected, the last button of this section, **ODD_EVEN_SEL**, becomes active and determines this. If *ODD/EVEN SEL* by Pin is selected instead, the selection to sample odd numbered channels or even numbered channels or even numbered channels or even numbered channels or even numbered channels this. If *ODD/EVEN SEL* by Pin is selected instead, the selection to sample odd numbered channels or even numbered channels or even numbered channels or even numbered channels or even numbered channels in interleave mode comes from the SPI or from the **INTERLEAVE_MUX** pin of the device. If *ODD/EVEN SEL* by SPI is selected, the last button of this section, **ODD_EVEN_SEL**, becomes active and determines this. If *ODD/EVEN SEL* by Pin is selected instead, the selection to sample odd numbered channels or even numbered channels in interleave mode comes from the state of the **INTERLEAVE_MUX** button in the *DEVICE PIN CONTROL* section of this tab.



GENERAL SET	JP	
RST (Soft Reset)	OFF	
EN_HIGH_ADDR	Disabled Regs ≥ 0xC8 Addr	
EN_EXT_REF	Disabled	\bigcirc
EN_INTERLEAVE	Enabled	\bigcirc
EN_MUX_REG	ODD/EVEN SEL by SPI	\bigcirc
ODD_EVEN_SEL	ODD	\bigcirc

Figure 60. GENERAL SETUP Section of Top Level Tab

The CUSTOM WRITE/READ section of the Top Level tab allows for custom writing to the serial interface of the ADS5296 as well as reading back register values. When a valid register address and value is provided the corresponding control will automatically update to reflect the current state of the device. In the example in Figure 61, the value of **PHASE_DDR** updated as a result of writing x8000 to reg42.

PHASE_DDR	00	•	\odot	ODD_EVEN_SEL ODD
DELAY_DATA_R	Tdr = Ops	•	\odot	CUSTOM WRITE/READ
DELAY_LCLK_R	Tcr = 159ps		\odot	Write Address × 42
DELAY_DATA_F	Tdf = 72ps	•	\odot	Write Data × 8000
DELAY_LCLK_F	Tcf = 120ps		\odot	Write Custom Register
				Custom Read Register
				Read Address × 0
				Read Data × 0
				Read Custom Register

Figure 61. CUSTOM WRITE/READ Example

5.3 Test Pattern Tab

The second sub-tab, shown in Figure 62, is *Test Pattern*. Within this tab, the user has the control of all the test patterns intrinsic to the device as described in the three sections of this tab: *PSEUDO-RANDOM BINARY SEQUENCE (PRBS)*, *CUSTOM FRAME CLOCK PATTERN*, *TEST PATTERN MODES*.



ADS5296 GUI in Detail

* ADS5295/ADS5296 GUI File Tools Check for GUI Updates Help **ADS5296 GUI** TEXAS INSTRUMENTS High Level Test Read Me First Test Pattern SIMULATION Top Level Digital Signal Processing Channel Filter Simulation Select Another Device RECORD/PLAYBACK COMMAND SEQUENCE Record Sequence PSEUDO-RANDOM BINARY SEQUENCE (PRBS) TEST PATTERN MODES PRBS_TP_EN Save Sequence TEST_PATT None • 0 PRBS_MODE_2 23-bit pattern Playback Sequence RAMP_PAT_RESET_VAL 0 ۲ PRBS_SEED_FROM_REG Clear Sequence (0x0000-0x3FFF) Recorded Sequence PRBS_SEED 0 🚔 🔘 Index Addr Data CUSTOM_DATA1 0 ÷ 0 (0x000000 - 0x7FFFFF) (0x0000-0x3FFF) TP_SOFT_SYNC CUSTOM_DATA2 0 TP_HARD_SYNC * 111 (0x0000-0x3FFF) CUSTOM FRAME CLOCK PATTERN address × 1C Data × 0 EN_FRAME_PAT ADCLKOUT 0 🔄 SCLK ----(0x0000-0x3FFF) SDATA - 0 1 0 0 SEN DEVICE STATUS Ready Idle

Figure 62. Test Pattern Tab

The *PRBS* section shows all its controls to be greyed an unselectable except for **PRBS_TP_EN** checkbox. Once this box is checked all the remaining controls are accessible as shown in Figure 63. The info buttons provide details on the definition of each control.

PSEUDO-RANDOM BINARY SEQUENCE (F	PRBS) —
PRBS_TP_EN	\bigcirc
PRBS_MODE_2 23-bit pattern	
PRBS_SEED_FROM_REG	\bigcirc
PRBS_SEED 0 🚔	\bigcirc
(0x000000 - 0x7FFFF)	
TP_SOFT_SYNC	\bigcirc
TP_HARD_SYNC	

Figure 63. PRBS Section Enabled

The *TEST PATTERN MODES* section contains commonly used test patterns under the **TEST_PATT** dropdown menu as shown in Figure 64. All of these patterns are generated internal to the ADS5296 device and provided on all channels simultaneously.



TEST_PATT	None 🗨 🦉
	✓ None
RAMP	RAMP PATTERN
	DUAL CUSTOM PATTERN
	SINGLE CUSTOM PATTERN
	DESKEW PATTERN
	SYNC PATTERN
L	
	(0x0000-0x3FFF)

Figure 64. TEST PATTERN MODES Section

5.4 Digital Signal Processing Tab

The Digital Signal Processing tab contains five sections as shown in Figure 65: CHANNEL AVERAGING, CHANNEL_GAIN, LOW FREQUENCY NOISE SUPPRESSION, SWAP ANALOG INPUTS, and INPUT/OUTPUT MAPPING.

ADS5295/ADS5296	5 GUI						
File Tools Check f	for GUI Upd	lates Help					
AP TEXAS INSTRUMEN	NTS			ADS	S5296 G	UI	
		Read	Me First			Hi	gh Level Test
Top Level		Test	Pattern	Digital Signa	l Processing	Channel Filter	SIMULATION
	ING					Y SWAP ANALOG	Simulation Select Another Device
EN_CHANNEL_	AVG	0	-CHANNEL_GAIN	0	NOISE SUPRESS	ION INPUT POLARITY	RECORD/PLAYBACK COMMAND SEQUENCE
AVG_OUT1	ZERO	-	GAIN CH1	0 dB 💌	LFNS_CH1	INVERT CH1	
AVG_OUT2	ZERO	-	GAIN CH2	0 dB 💌	LFNS_CH2	INVERT CH2	Save Sequence
AVG_OUT3	ZERO	-	GAIN CH3	0 dB 💌	LFNS_CH3	INVERT CH3	Playback Sequence
AVG_OUT4	ZERO	-	GAIN CH4	0 dB 💌	LFNS_CH4	INVERT CH4	Recorded Sequence
AVG_OUT5	ZERO	-	GAIN CH5	0 dB 💌	LFNS_CH5	INVERT CH5	Index Addr Data
AVG_OUT6	ZERO	-	GAIN CH6	0 dB 💌	LFNS_CH6	INVERT CH6	
AVG_OUT7	ZERO	-	GAIN CH7	0 dB 🗨	LFNS_CH7	INVERT CH7	
AVG_OUT8	ZERO	-	GAIN CH8	0 dB	LFNS_CH8	INVERT CH8	۲
		PING					
			ENA	ABLE MAPPING	\bigcirc		address × 29 Data × 0
N N	MAP LVDS O	UTPUTS 1-41	FO INPUT CH1-4	MA	P LVDS OUTPUTS 5-8 TO	INPUT CH5-8	
MAP_CH	H13_TO_OU	T 1/OUT 2	Input Channel IN1	MAP_CH57	TO_OUT 5/OUT 6 Inp	out Channel IN7 👻	
MAP_CH	H13_TO_OU	T 3/OUT 4	Input Channel IN1	MAP_CH57	TO_OUT 7/OUT 8 Inp	out Channel IN7 💌	SEN - 0
							Ready Idle

Figure 65. Digital Signal Processing Tab

59



ADS5296 GUI in Detail

www.ti.com

The *CHANNEL AVERAGING* function is enabled by the checkbox labeled **EN_CHANNEL_AVG** as shown in Figure 66. Once checked, the drop-down menus within the section become un-greyed and active as shown. The drop-down menu shown in Figure 66 corresponds to the choices available to output onto OUT1 of the device.

CHANNEL AVE	- CHANNEL AVERAGING							
EN_CHAN	EN_CHANNEL_AVG 🔽 🛛 🔘							
AVG_OUT1	ZERO 💌							
AVG_OUT2	✓ ZERO							
AVG OUT3	ADC CH1							
	AVG ADC CH1,2							
AVG_OUT4	AVG ADC CH1,2,3,4							
AVG_OUT5	ZERO 💌							
AVG_OUT6	ADC CH7							
AVG_OUT7	ADC CH6							
AVG_OUT8	ZERO 💌							

Figure 66. Digital Signal Processing Tab

With Zero selected from the drop-down menu, the output to Channel 1 is fixed at maximum ADC code. With *ADC CH1* selected, the normal Channel 1 output is captured as in the case when channel averaging is disabled. With *AVG ADC CH1,2* selected, the Channel 1 output now contains the averaged output Channel 1 and Channel 2 which improves SNR by approximately 4.6 dB. Finally, with *AVG ADC CH1,2,3,4* selected the output of Channel 1 contains the average of the four channels which improves SNR by 5.4 dB typically. (*Note: pressing the info button in this section shows the graphic in Figure 67. This table, from the datasheet, shows only the averaging options for each output, which is either a twochannel average or a four-channel average. Not shown in the table are the two other options appearing the GUI drop-down menus, ZERO and ADC CHx, which represents the actual design implementation.*)

PRBS Enable Help										
Table 12. Using Channel Averaging										
AVERAGED CHANNELS	OUTPUT WHERE AVERAGED DATA ARE AVAILABLE AT	REGISTER SETTINGS								
1, 2	OUT1	Set AVG_OUT1 = 10 and EN_CHANNEL_AVG = 1								
1, 2	OUT3	Set AVG_OUT3 = 11 and EN_CHANNEL_AVG = 1								
3, 4	OUT4	Set AVG_OUT4 = 10 and EN_CHANNEL_AVG = 1								
3, 4	OUT2	Set AVG_OUT2 = 11 and EN_CHANNEL_AVG = 1								
1, 2, 3, 4	OUT1	Set AVG_OUT1 = 11 and EN_CHANNEL_AVG = 1								
1, 2, 3, 4	OUT4	Set AVG_OUT4 = 11 and EN_CHANNEL_AVG = 1								
5, 6	OUT5	Set AVG_OUT5 = 10 and EN_CHANNEL_AVG = 1								
5, 6	OUT7	Set AVG_OUT7 = 11 and EN_CHANNEL_AVG = 1								
7, 8	OUT8	Set AVG_OUT8 = 10 and EN_CHANNEL_AVG = 1								
7, 8	OUT6	Set AVG_OUT6 = 11 and EN_CHANNEL_AVG = 1								
5, 6, 7, 8	OUT5	Set AVG_OUT5 = 11 and EN_CHANNEL_AVG = 1								
5, 6, 7, 8	OUT8	Set AVG_OUT8 = 11 and EN_CHANNEL_AVG = 1								

Figure 67. Channel Averaging Info Button



The *INPUT/OUTPUT MAPPING* section allows the user to remap the analog input channels to any of the digital output channels. The implementation in silicon allows for all combinations of mapping. However, because each combination requires a unique firmware or DLL configuration, the GUI limits the number of combinations available in mapping. To un-grey and enable this section check the **ENABLE MAPPING** checkbox as shown in Figure 68.

ENA	ABLE MAPPING 🔽 💿
MAP LVDS OUTPUTS 1-4 TO INPUT CH1-4	MAP LVDS OUTPUTS 5-8 TO INPUT CH5-8
MAP_CH1234_TO_OUT 1 Input Channel IN1	MAP_CH5678_TO_OUT 5 Input Channel IN8
MAP_CH1234_TO_OUT 2 Input Channel IN1	MAP_CH5678_TO_OUT 6 Input Channel IN8
MAP_CH1234_TO_OUT 3 Input Channel IN1	MAP_CH5678_TO_OUT 7 Input Channel IN8
MAP_CH1234_TO_OUT 4 Input Channel IN1	MAP_CH5678_TO_OUT 8 Input Channel IN8

Figure 68. INPUT/OUTPUT MAPPING with EN_INTERLEAVE = 0

The default state of this section shows that output channels 1–4 have mapped the signal that is sampled at analog input channel 1, while channels 5–8 have mapped the signal that is sampled at analog input channel 8. This menu applies if interleaving is disabled. If interleaving is enabled on the *Top Level* tab, then the mapping options reflects this as shown in Figure 69.

INPUT/OUTPUT MAPPING		
E	NABLE MA	APPING 📝 💿
MAP LVDS OUTPUTS 1-4 TO INPUT CH1-4		MAP LVDS OUTPUTS 5-8 TO INPUT CH5-8
MAP_CH13_TO_OUT 1/OUT 2 Input Channel IN1	-	MAP_CH57_TO_OUT 5/OUT 6 Input Channel IN7
MAP_CH13_TO_OUT 3/OUT 4 Input Channel IN1	1 🔽	MAP_CH57_TO_OUT 7/OUT 8 Input Channel IN7

Figure 69. INPUT/OUTPUT MAPPING with EN_INTERLEAVE = 1

The remaining sections of the *Digital Signal Processing* tab are straightforward and explained by the info buttons provided.

5.5 Channel Filter Tab

The last tab is *Channel Filter* and contains the controls for the decimation filters as well as the integrated high pass filters. As shown in Figure 70, the controls have interdependencies, reflecting the actual silicon implementation.



ADS5296 GUI in Detail

🚸 High Sp	peed Data	a Converte	r Pro					T CL	I.I.I.TRALES	
File Inst	rument O	ptions D	ata Capture Options Test Op	tions Devic	e GUI Options	Help				
4	Texas Instru	MENTS			Hig	jh Spe	ed Data Cor	nverte	er Pro v2.10	
	ADC DAC									ADS5296 GUI
	ADS5296			Re	ad Me First				High L	evel Test
	Capture		Top Level	Te	est Pattern		Digital Signal Processin	ng	Channel Filter	SIMULATION
Test Sel	ection		CHANNEL 1	Сн	IANNEL 2		CHANNEL 3		CHANNEL 4	Simulation
Sing	gle Tone	-	USE_FILTE Pre-stored/ Custom Coeff Use Pre-Stored	R Pre-sto Custon	red/ 1 Coeff Use Pre	E_FILTER	Pre-stored/ Custom Coeff Use Pre-St	FILTER	Pre-stored/ Custom Coeff Use Pre-Stored	RECORD/PLAYBACK COMMAND SEQUENCE
SNR	Value 0.00	dBFs	SEL_ODD_TAP_CH 24-tap	SEL_C	DD_TAP_CH 2	4-tap 💌	SEL_ODD_TAP_CH 24-t	tap 💌	SEL_ODD_TAP_CH 24-tap 👻	Record Sequence
SFDR	0.00	dBc	FILTER_TYPE_CH SET1	FILTE	R_TYPE_CH	SET1 💌	FILTER_TYPE_CH SE	ET1 🔻	FILTER_TYPE_CH SET1 -	Save Sequence
THD	0.00	dBFs	DEC_RATE_CH No Dec.	- V DEC	RATE_CH N	lo Dec 💌	DEC_RATE_CH No D	Dec 💌	DEC_RATE_CH No Dec 👻	Playback Sequence
ENOB	0.00	Bits	HPF EN C	н 🔲	HP	F EN CH	HPF	EN CH	HPF EN CH	Playback Sequence
Fund. Worst Spur	0.00	dBFs	HPF_CORNER_CH 2	HPF_(CORNER_CH	2	HPF_CORNER_CH	2	HPF_CORNER_CH 2	Recorded Sequence Clear Sequence
HD2	dBFs	Hz	CHANNEL 5	Сн	ANNEL 6		CHANNEL 7		CHANNEL 8	Index Addr Data 🔺
HD3	0.00	0.00E+0	Pre-stored/ USE_FILTE	R Pre-sto	red/ USE	E_FILTER	Pre-stored/	FILTER	Pre-stored/	
HD4 HD5	0.00	1.00E+6	Custom Coeff Use Pre-Stored	Custon	Coeff Use Pre-	-Stored	Custom Coeff Use Pre-St	orea 💌	Custom Coeff Use Pre-Stored	
HD6			SEL_ODD_TAP_CH 24-tap	SEL_C	DD_TAP_CH 2	4-tap 💌	SEL_ODD_TAP_CH 24-t	ap 💌	SEL_ODD_TAP_CH 24-tap	< III >
M1			FILTER_TYPE_CH SET1	FILTE	R_TYPE_CH	SET1 💌	FILTER_TYPE_CH SE	ET1 💌	FILTER_TYPE_CH SET1 -	
M2			DEC_RATE_CH No Dec.	DEC_	RATE_CH N	lo Dec 💌	DEC_RATE_CH No D	Dec 💌	DEC_RATE_CH No Dec	address × 38 Data × 0
Delta Test Para	neters		HPF_EN_C	н 📃	HP	F_EN_CH	HPF_E	EN_CH	HPF_EN_CH	DIGITAL WAVEFORM GRAPH-WRITE
Auto Ca	lculation of	of	HPF_CORNER_CH 2	HPF_C	CORNER_CH	2	HPF_CORNER_CH	2	HPF_CORNER_CH 2	
Coherer	nt Frequen	cies	EN_DIG_FILTER							
Analysis W	indow (sai	mpies)								SDATA - 0 1 0
ADC Outp	ut Data R	ate								SEN - 0
8	80M									Deset Channels
ADC Input	Target Fr	equency								Select
15.49	926758M									
										DEVICE STATUS
										Working Send TSW Parameters
		Firmwar	e Version = "0.2"			TSW 1400 B	pard = TIWAKA6L		Interface	Type = ADC_FIRMWARE
Clear AD	C Plot				5/17/2013 1	:54:28 PM	Build - 04/30/2013	CON	NECTED	Texas Instruments

Figure 70. Channel Filter Tab

Checking the **EN_DIG_FILTER** box causes the **USE_FILTER** control to become un-greyed and enabled for all eight channels as shown in Figure 71.



Na Lligh Sp	and Data	Converte	r Dro							
File Instr	rument O	ptions D	ata Capture Options Test Opt	ions Devic	e GUI Options He	elp				
Jia 1	TEXAS	•							-	
Y I	INSTRUI	MENTS			High	Spe	ed Data Conv	erter	Pro v2.10	
			ADC			>	DAC			ADS5296 GUI
A	ADS5296			Rei	ad Me First				High	Level Test
(Capture		Top Level	Te	est Pattern		Digital Signal Processing		Channel Filter	SIMULATION
Test Sele	ection		CHANNEL 1	СН	IANNEL 2		CHANNEL 3		CHANNEL 4	Simulation
Sing	jle Tone	•	Pre-stored/ Custom Coeff Use Pre-Stored	Pre-sto Custom	red/ Coeff Use Pre-Stor	ed 🖵	Pre-stored/ Custom Coeff Use Pre-Stored	id 🔻 O	re-stored/ ustom Coeff Use Pre-Stored	RECORD/PLAYBACK COMMAND SEQUENCE
5NR	Value 0.00	Unit dBFs	SEL_ODD_TAP_CH 24-tap	SEL_C	DD_TAP_CH 24-tap		SEL_ODD_TAP_CH 24-tap	v S	EL_ODD_TAP_CH 24-tap	Record Sequence
SFDR	0.00	dBc	FILTER_TYPE_CH SET1	▼ FILTE	R_TYPE_CH SET	1 💌	FILTER_TYPE_CH SET1	. 💌 F	FILTER_TYPE_CH SET1	Save Sequence
SINAD	0.00	dBFs	DEC_RATE_CH No Dec	▼ DEC_	RATE_CH No De	C 💌	DEC_RATE_CH No Dec.	💌 🛛	DEC_RATE_CH No Dec 💌	Playback Sequence
ENOB	0.00	Bits	HPF_EN_C	1	HPF_EN	СН 📃	HPF_EN_	СН	HPF_EN_CH	Clear Services
Funa. Worst Spur	0.00	dBFs	HPF_CORNER_CH 2	HPF_C	CORNER_CH	2	HPF_CORNER_CH 2	H	IPF_CORNER_CH 2	Recorded Sequence
HD2	dBFs	Hz	CHANNEL 5	СН	ANNEL 6	TER 🗐	CHANNEL 7		CHANNEL 8	Index Addr Data
HD3 HD4	0.00	0.00E+0 1.00E+6	Pre-stored/ Custom Coeff Use Pre-Stored	Pre-sto	red/ Coeff Use Pre-Stor	ed 👻	Pre-stored/ Custom Coeff Use Pre-Stored	d 🔻 Pr	re-stored/ ustom Coeff Use Pre-Stored 💌	
HDS HD6	0.00	1.00E+6	SEL_ODD_TAP_CH 24-tap	SEL_C	DD_TAP_CH 24-tap	•	SEL_ODD_TAP_CH 24-tap	- S	EL_ODD_TAP_CH 24-tap	· · ·
			FILTER_TYPE_CH SET1	▼ FILTE	R_TYPE_CH SET	1 💌	FILTER_TYPE_CH SET1	- F	ILTER_TYPE_CH SET1	
V1 V12			DEC_RATE_CH No Dec	▼ DEC_F	RATE_CH No De	c 💌	DEC_RATE_CH No Dec.	💌 D	DEC_RATE_CH No Dec	address × 29 Data × 2
Delta			HPF_EN_CH	1	HPF_EN	LCH 📃	HPF_EN_(СН 📃	HPF_EN_CH	
Test Paran	neters	f	HPF_CORNER_CH 2	HPF_C	CORNER_CH	2	HPF_CORNER_CH 2	н	IPF_CORNER_CH 2	
Coheren	t Frequent	xies .								
Analysis W	indow (san	nples)								
ADC Outp	ut Data Ra	te								SEN - 0
8	0M									Reset Channels
ADC Input	Target Fre	quency								Select
15,499	920758IVI									
										DEVICE STATUS
										Idle
		Firmwar	e Version = "0.2"		TSW 1400 Board = TIWAKA6L				Interface	• Type = ADC_FIRMWARE
Waiting fo	or user in	put			5/17/2013 2:00:	59 PM	Build - 04/30/2013	CONNE	ECTED Id	e Texas Instruments

Figure 71. EN_DIG_FILTER = 1

At this point, the user can invoke the high pass filter for any channel by checking the box **HPF_EN_CH**. The box just below labeled **HPF_CORNER_CH** becomes active, as shown in Figure 72, and the corner frequency can be set to one of sixteen values, with zero being the highest corner frequency available.

CHANNEL 5 Pre-stored/ Custom Coeff Use P	JSE_FILTER
SEL_ODD_TAP_CH	24-tap 💌
FILTER_TYPE_CH	SET1 👻
DEC_RATE_CH	No Dec 💌
HPF_CORNER_CH	HPF_EN_CH

Figure 72. Channel 5 High Pass Filter Enabled

The ADS526's digital processing block includes the option to filter and decimate the ADC outputs digitally. Various decimation rates and filters are supported including decimation by 2, 4, or 8, low-pass, high-pass, and band-pass filters. To invoke this block the **USE_FILTER** box must be checked, thus, enabling all controls associated with the digital and decimation filters as shown in Figure 73.

CHANNEL 1 Pre-stored/ Custom Coeff Use Pr	JSE_FILTER 🔽 re-Stored 🖵		
SEL_ODD_TAP_CH	24-tap 💌		
FILTER_TYPE_CH	SET1 👻		
DEC_RATE_CH	No Dec 💌		
ŀ	HPF_EN_CH		
HPF_CORNER_CH	2		

Figure 73. Channel 1 Digital Filter Enabled

The user has the option to use pre-defined filter coefficients or define custom coefficients. When Use Pre-Stored Filter Coeff is selected, one of six pre-defined filter types, depending on the state of FILTER_TYPE_SEL, will be configured. The Digital Filters Table of the datasheet describes these configurations and is available through the info button on this tab. In addition, the six pre-defined filters are presented graphically at the bottom of the Channel Filter tab when the channel chosen to view (from View Pre-Stored/Custom Filter Coeff section at bottom left) has Use Pre-Stored selected.



Figure 74. Channel 1 Pre-Stored Digital Filter Enabled

If, instead, *Enable Custom Filter* is selected, then all controls associated with the pre-defined filters become inactive as shown in Figure 75. In addition, the graphs of the pre-stored filters are replaced with the twelve registers that hold the twelve, 12-bit, signed coefficients for one custom filter.



🖗 High Speed Data Converter Pro									×		1m			
File Instrument Options Data Capture Options Test Options Device GUI Options Help														
High Speed Data Converter Pro v2.10														
ADC					DAC						ADS5296 GUI			
ADS5296 🛃				Me First					High Level Test					
Canture		Top Level		Test P	Test Pattern			Digital Signal Processing			Channel Filter SIMULATION			
Test Sele	ction		CHANNEL 1		CHANN	CHANNEL 2		CHANNEL 3		CHANNEL 4		Simulation		
Sing	le Tone	•	Pre-stored/ Custom Coeff Ena	USE_FILTER	Pre-stored/ Custom Co	USE eff Use Pre-	E_FILTER 📄 -Stored 🖃	Pre-stored/ Custom Co	eff Use P	re-Stored 💌	Pre-stored/ Custom Coeff	USE_FILTER USE_FILTER	RECORD/PLAYBACK COMMAND SEQUENCE	
SNR	0.00	dBFs	SEL_ODD_TAP_CH	H 24-tap	SEL_ODD	TAP_CH 24	4-tap 💌	SEL_ODD	TAP_CH	24-tap 💌	SEL_ODD_TAP	_CH 24-tap 💌	Record Sequence	
SFDR	0.00	dBc	FILTER_TYPE_CH	SET1	FILTER_T	YPE_CH	SET1 💌	FILTER_T	YPE_CH	SET1 💌	FILTER_TYPE_	CH SET1 💌	Save Sequence	
SINAD	0.00	dBFs	DEC_RATE_CH	Dec. by 4	DEC_RAT	E_CH D	ec. by 4 💌	DEC_RAT	E_CH	Dec. by 4 💌	DEC_RATE_CH	l Dec. by 4 💌	Playback Sequence	
ENOB Fund	0.00	Bits		HPF_EN_CH		HPI	F_EN_CH		ł	IPF_EN_CH 📃		HPF_EN_CH	Clear Sequence	
Worst Spur	0.00	dBFs	HPF_CORNER_CH	2	HPF_COR	NER_CH	2	HPF_COR	NER_CH	2	HPF_CORNER	_CH 2	Recorded Sequence	
HD2 HD3	dBFs 0.00	Hz 0.00F+0	USE FILTER		CHANN	CHANNEL 6		CHANNEL 7 USE_FILTER		CHANNEL 8 USE_FILTER		Index Addi Data		
HD4	4 0.00 1.00E+6		Pre-stored/ Custom Coeff Use Pre-Stored 💌		 Pre-stored/ Custom Cost 	Pre-stored/ Custom Coeff Use Pre-Stored 💌		Pre-stored/ Custom Coeff Use Pre-Stored 💌			Pre-stored/ Custom Coeff Use Pre-Stored 💌			
HD5 HD6	0.00	1.00E+6	SEL_ODD_TAP_CH	l 24-tap	SEL_ODD	SEL_ODD_TAP_CH 24-tap		SEL_ODD_TAP_CH 24-tap			SEL_ODD_TAP	_CH 24-tap 💌		
			FILTER_TYPE_CH	SET1	FILTER_T	(PE_CH	SET1 💌	FILTER_T	YPE_CH	SET1 💌	FILTER_TYPE_	CH SET1 💌		
M2			DEC_RATE_CH	Dec. by 4	DEC_RATE	E_CH De	ec. by 4 💌	DEC_RAT	E_CH	Dec. by 4 💌	DEC_RATE_CH	Dec. by 4 💌	address × 38 Data × 2	
Delta	otorc			HPF_EN_CH		HPF	F_EN_CH		H	IPF_EN_CH 📃		HPF_EN_CH	DIGITAL WAVEFORM GRAPH-WRITE	
Auto Cal	culation of	F	HPF_CORNER_CH	8	HPF_CORI	NER_CH	2	HPF_COR	NER_CH	2	HPF_CORNER_	CH 2		
Coheren	t Frequenc	ies	EN_DIG_FILTER	Custom Filt /	Addr × 5A	Custom	Filt Addr × 5	в	Custom Fil	Addr × 5C	Custom Fil	t Addr 🛛 × 5D		
Analysis Window (samples)		View Pre-stored/	N4 N3	N2 N1	N4	N3 N2	N1	N4 N3	N2 N	1 N4 N3	3 N2 N1	SDATA - 0 1 0		
ADC Output Data Rate		Custom Filter Coeff	×8 ×0	×0 ×0		×0 ×0		×8 ×0	×0 ×() <u>×8</u> ×0	×0 ×0	SEN - 0		
80M		CH1 CH2 CH3	Custom Filt /	Addr × 5E	Custom	Filt Addr × 5	F	Custom Fil	Addr × 60	Custom Fil	t Addr ×61	Reset Channels		
ADC Input	Target Fre	quency	• • •	N4 N3	N2 N1	N4	N3 N2	N1	N4 N3	N2 N	1 N4 N3	3 N2 N1	Select	
13.49920738101		CH4 CH5 CH6									Save/Load Custom Filter Coeffs			
			CH7 CH8	Custom Filt /	Addr × 62	Custom	Filt Addr × 6	Custom Filt Addr × 64			Custom Fil	t Addr × 65	Select an Option	
				×8 ×0	×0 ×0	×8	×0 ×0	×0	×8 ×0	×0 ×(x8 ×0	×0 ×0	Ready Idle	
Firmware Version = "0.2"						TSW 1400 Board = TIWAKA6L						Interface Type = ADC_FIRMWARE		
Waiting for user input					5	5/17/2013 3:10:32 PM Build - 04/30/2013 CONI						Idle	TEXAS INSTRUMENTS	

Figure 75. Channel 1 Custom Digital Filter Enabled

Because of the large number of inputs required to define all eight custom filters ($8 \times 12 = 96$ coefficients), the GUI provides a means for loading coefficients from a text file, saving coefficients to a text file, and resetting filter coefficient values. This control is located in the bottom right corner of *Channel Filter* tab. As shown in Figure 76, *Reset Channels* can be applied to only Pre-stored Filters, only Custom Filters, or to all filters.



Figure 76. Reset Channels on Channel Filter Tab

The *Save/Load Custom Filter Coeffs* drop-down menu, as shown in Figure 77, can be used to save the currently displayed channel's custom coefficients to a file or all channels' custom coefficients to a file.



Reset Channels							
Reset All 💌							
Save/Load Custom Filter Coeffs							
Select an Option							
✓Select an Option							
Save Filter Coeffs to File (Current Filter)							
Save Filter Coeffs to File (All Filters)							
Load Filter Coeffs from File (Current Filter)							
Load Filter Coeffs from File (All Filters)							
- Reset All Custom Filters							



Likewise, one can load the custom coefficients for the current channel or for all channels. The current channel is indicated on the lower left corner in the *View Pre-stored/Custom Filter Coeff* section shown in Figure 78. Only those channels whose **USE_FILTER** bit are enabled are active, and thus, available for viewing.

🖓 High Speed Data Converter Pro											
File Instrument Options Data Capture Options Test Options Device GUI Options Help											
High Speed Data Converter Pro v2.10											
ADC		L L	DAC	ADS5296 GUI							
ADS5296	Read	Me First		High Lev	High Level Test						
Capture Top Level	Tes	t Pattern	Digital Signal Processing	Channel Filter	SIMULATION						
Test Selection CHANNEL 1	CHA	NNEL 2	CHANNEL 3	CHANNEL 4	Simulation						
Single Tone Pre-stored/ Custom Coeff Ena	USE_FILTER V	USE_FILTER ♥ d/ Coeff Enable Custom ▼	USE_FILTER V Pre-stored/ Custom Coeff Enable Custom	USE_FILTER V Pre-stored/ Custom Coeff Enable Custom	RECORD/PLAYBACK COMMAND SEQUENCE						
Value Unit	H 24-tap 💌 SEL OD	D TAP CH 24-tap	SEL ODD TAP CH 24-tap	SEL ODD TAP CH 24-tap	Record Sequence						
SFDR 0.00 dBc FILTER TYPE CH	SET1 FILTER	TYPE CH SET1	FILTER TYPE CH SET1	FILTER TYPE CH SET1	Save Sequence						
THD 0.00 dBFs SINAD 0.00 dBFs DEC_RATE_CH	Dec. by 2 V DEC_R	ATE_CH Dec. by 2	DEC_RATE_CH Dec. by 2	DEC_RATE_CH Dec. by 2 💌	Playback Sequence						
ENOB 0.00 Bits	HPF_EN_CH	HPF_EN_CH	HPF_EN_CH	HPF_EN_CH							
Fund. 0.00 dBFs HPF_CORNER_CH	1 2 HPF_CC	DRNER_CH 2	HPF_CORNER_CH 2	HPF_CORNER_CH 2	Recorded Sequence						
HD2 dBFs Hz CHANNEL 5	CHAI	NNEL 6	CHANNEL 7	CHANNEL 8	Index Addr Data 🔺						
HD3 0.00 0.00E+0 Pre-stored/ HD4 0.00 1.00E+6 Outtom Cooff Enal	USE_FILTER	d/ Enable Custom	Pre-stored/ Cutom Coeff Enable Custom	Pre-stored/ Cuttom Coeff Enable Custom							
HD5 0.00 1.00E+6	H 24-tap	D_TAP_CH 24-tap	SEL_ODD_TAP_CH 24-tap	SEL_ODD_TAP_CH 24-tap	-						
FILTER_TYPE_CH	SET1 - FILTER	TYPE_CH SET1 -	FILTER_TYPE_CH SET1 -	FILTER_TYPE_CH SET1	4						
M1 DEC_RATE_CH	Dec. by 2 V DEC_RA	ATE_CH Dec. by 2 💌	DEC_RATE_CH Dec. by 2 👻	DEC_RATE_CH Dec. by 2 💌	address u. or. Data u. 2000						
Delta	HPF EN CH	HPF EN CH	HPF EN CH	HPF EN CH							
Test Parameters HPF_CORNER_CH	HPF_CORNER_CH 2 HPF_CC		HPF_CORNER_CH 2	HPF_CORNER_CH 2							
Auto Calculation of Coherent Frequencies	Custom Filt Addr × 5A	Custom Filt Addr × 5	B Custom Filt Addr × 5C	Custom Filt Addr × 5D	Salk-						
Analysis Window (samples)	N4 N3 N2 N1	N4 N3 N2	N1 N4 N3 N2 N1	N4 N3 N2 N1	SDATA-						
ADC Output Data Rate	×8 ×0 ×0 ×1	×8 ×0 ×0	×0 ×8 ×0 ×0 ×0	×8 ×0 ×0 ×0	SEN - 0						
80M CH1 CH2 CH3	Custom Filt Addr × 5E	Custom Filt Addr × 5	F Custom Filt Addr × 60	Custom Filt Addr ×61							
ADC Input Target Frequency 🕘 🔘	N4 N3 N2 N1	N4 N3 N2	N1 N4 N3 N2 N1	N4 N3 N2 N1	Reset All						
15.49926758M CH4 CH5 CH6	×8 ×0 ×0 ×0	×8 ×0 ×0	×0 ×8 ×0 ×0 ×0	×8 ×0 ×0 ×0	Save/Load Custom Filter Coeffs						
000	Custom Filt Addr × 62	Custom Filt Addr ×6	3 Custom Filt Addr ×64	Custom Filt Addr ×65Select an Option							
CH7 CH8	N4 N3 N2 N1 ×8 ×0 ×0 ×0	N4 N3 N2 ×8 ×0 ×0	N1 N4 N3 N2 N1 ×0 ×8 ×0 ×0 ×0	N4 N3 N2 N1 ×8 ×0 ×1 ×0	DEVICE STATUS						
Firmware Version = "0.2"		TSW 1400 B	oard = TIWAKA6L	Interface Type = ADC_FIRMWARE							
Waiting for user input 5/17/2013 3:55:51 PM Build - 04/30/2013 CONNECTED Idle 🚸 TEXAS INSTRU											

Figure 78. View Filter Coeffs





50



Figure 79. ADS5296 Schematic, Sheet 1 of 9

.118





Figure 80. ADS5296 Schematic, Sheet 2 of 9











ADS5296 EVM Schematics

www.ti.com











Figure 83. ADS5296 Schematic, Sheet 5 of 9







Figure 84. ADS5296 Schematic, Sheet 6 of 9


























7 ADS5296 EVM Bill of Materials

Table 2. ADS5296 EVM Bill of Materials

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
8	C1, C3, C5, C25, C29, C42, C102, C230	10UF	AVX	TAJB106K016RNJ	CAP TANT 10UF 16V 10% 1210
90	C10, C11, C12, C18, C20, C26, C27, C28, C30, C41, C43, C44, C45, C46, C49, C50, C59, C60, C61, C62, C63, C70, C78, C79, C83, C85, C93, C99, C100, C124, C125, C126, C191, C192, C193, C195, C196, C205, C206, C207, C209, C210, C219, C220, C221, C223, C224, C231, C233, C234, C235, C236, C237, C239, C240, C242, C243, C244, C245, C246, C247, C248, C249, C257, C258, C259, C260, C261, C262, C265, C266, C268, C269, C271, C272, C276, C277, C278, C279, C280, C282, C283, C285, C286, C288, C289, C290, C291, C292	0.1uF	AVX	06035C104JAT2A	CAP CER .10UF 50V X7R 10% 0603
1	C149	10nF	MURATA	GRM188R71H103KA01D	CAP 10000PF 50V CERM X7R 0603
2	C150, C153	47pF	MURATA	GRM1885C1H470JA01D	CAP CERAMIC 47PF 50V 0603 SMD
1	C151	4.7uF	AVX	TAJA475K020R	CAP TANTALUM 4.7UF 20V 10% SMD
2	C152, C154	0.1UF	TAIYO YUDEN	GMK105BJ104KV-F	0.1uF 35V X5R 0402
4	C187, C201, C215, C229	33pF	MURATA	GRM1885C1H330JA01D	CAP CER 33PF 50V X7R 10% 0603
9	C2, C4, C6, C40, C91, C97, C101, C232, C294	1uF	AVX	0603YC105KAT2A	CAP CER 1.0UF 16V X7R 10% 0603
8	C238, C267, C270, C273, C281, C284, C287, C293	6.8 pF	MURATA	GRM1885C1H6R8DZ01D	CAP CER 6.8PF 50V NP0 0603
16	C51, C52, C53, C54, C55, C56, C57, C58, C77, C80, C84, C86, C87, C88, C89, C90	220pF	AVX	06035A221FAT2A	DNI; CAP CERM 220PF 1% 50V NP0 0603
4	C64, C188, C202, C216	2.2uF	TDK	C1608X5R1E225K	2.2UF 25V X5R 10% 0603
4	C65, C194, C208, C222	0.1uF	MURATA	GRM1885F51E104ZA01D	DNI
16	C66, C67, C71, C72, C197, C198, C199, C200, C211, C212, C213, C214, C225, C226, C227, C228	0.001uF			DNI
8	C68, C69, C189, C190, C203, C204, C217, C218	10nF	TDK	C1608X7R1H103K	.01uF, 50V, 10%, X7R, 0603
2	C92, C98	100PF	Panasonic	ECH-U1C101JX5	CAP FILM 100PF 16VDC 0603
1	D1	LNJ308G8PRA	PANASONIC	LNJ308G8PRA	LED, GREEN, SMT-0603
1	D2	MBRB2515L	ON Semiconductor	MBRB2515LT4GOSCT-ND	DIODE SCHOTTKY 15V 25A D2PAK
1	J1	RED	ALLIED ELECTRONICS	ST-351A	Banana Female Red
1	J1_1	T POINT R (RED)	Keystone Electronics	5000	
1	J13	USB_MINI_AB	JAE	DX3R005HN2E700	USB_MINI_AB
11	J14, J15, J16, J17, J18, J19, J20, J21, J22, J31, J33	SMA	SAMTEC	SMA-J-P-H-ST-TH1	JACK PANEL MOUNT SMA
1	J2	BLK	ALLIED ELECTRONICS	ST-351B	Banana Female Black
1	J2_1	T POINT R (BLK)	Keystone Electronics	5001	
4	J27, J28, J29, J30	SMA	Johnson	1420-0711-821	Side Mounted SMA
18	J34, J35, J36, J37, J38, J39, J40, JP2, JP3, JP4, JP14, TP12, TP13, TP14, TP15, TP16, TP17, TP20	HEADER 3POS .1 CTR	ANY	JUMPER,3P,.100CC	JUMPER,3P,.100CC
1	J8	QTH-060-02-F-D-A	SAMTEC	QTH-060-02-F-D-A	High speed connector
1	JP1	HEADER_1x2_100_430L	SAMTEC	HMTSW-102-07-G-S240	CONN HEADER 2POS .100" T/H GOLD
8	L10, L11, L71, L72, L77, L78, L83, L84	10nH	Stewart	EXC-ML32A680U	DNI
8	L4, L6, L73, L74, L79, L80, L85, L86	0.043uH	Stewart	EXC-ML32A680U	DNI
64	L7, L8, L9, L69, L70, L75, L76, L81, L82, R3, R50, R72, R73, R197, R198, R199, R200, R201, R202, R203, R207, R208, R209, R210, R283, R284, R285, R286, R287, R288, R289, R304, R312, R313, R318, R334, R335, R340, R356, R357, R362, R376, R377, R380, R381, R382, R384, R384, R386, R390, R391, R392, R393, R394, R395, R396, R397, R398, R399, R402, R403, R404, R405	0 ohm	PANASONIC	ERJ-3GEY0R00V	RESISTOR,SMT,0603,0 OHM,5%,ZERO OHM JUMPER



Table 2. ADS5296 EVM Bill of Materials (continued)

Qty	Reference Designator	Value	Manufacturer	Part Number	Description
2	R100, R106	5.1 ohm	VISHAY	CRCW06035R10FKEA	RES 5.10 OHM 1/10W 1% 0603 SMD
2	R101, R107	1K OHM	TYCO ELECTRONICS	CRG0603F1K0	RES 1.00K OHM 1/10W 1% 0603
2	R186, R187	0 ohm	PANASONIC	ERJ-2GE0R00X	RES 0 OHM 1/16W 1% 0402 SMD
17	R35, R46, R85, R86, R87, R93, R94, R95, R96, R153, R159, R160, R161, R163, R164, R171, R172	10 ohm	PANASONIC	ERJ-3GEYJ100V	RES 10.0 OHM 0603 SMD
36	R36, R37, R38, R39, R40, R41, R42, R43, R51, R57, R68, R74, R75, R80, R92, R97, R130, R131, R132, R134, R169, R170, R181, R314, R315, R319, R324, R325, R326, R327, R336, R337, R341, R358, R359, R363	24.9 Ohm	PANASONIC	ERJ-3EKF24R9V	RES 24.9 OHM 1/10W 1% 0603 SMD
3	R45, R48, R401	100	Panasonic	ERJ-3GEYJ101V	RES 100 OHM 1/10W 5% 0603 SMD
2	R53, R56	10K Ohm	PANASONIC	ERJ-3EKF1002V	RES 10.0K OHM 1/10W 1% 0603 SMD
16	R55, R69, R320, R321, R342, R343, R346, R347, R348, R349, R364, R365, R368, R369, R370, R371	24.9 Ohm	PANASONIC	ERJ-3EKF24R9V	DNI; RES 24.9 OHM 1/10W 1% 0603 SMD
16	R58, R66, R305, R306, R307, R311, R322, R323, R329, R333, R344, R345, R351, R355, R366, R367	49.9 Ohm	PANASONIC	ERJ-3EKF49R9V	DNI; RES 49.9 OHM 1/10W 1% 0603 SMD
16	R59, R60, R61, R62, R63, R64, R65, R67, R127, R128, R129, R133, R140, R141, R142, R143	12.4 Ohm	PANASONIC	ERJ-3EKF12R4V	RES 12.4 OHM 1/10W 1% 0603 SMD
5	R6, R54, R328, R350, R372	49.9 Ohm	PANASONIC	ERJ-3EKF49R9V	RES 49.9 OHM 1/10W 1% 0603 SMD
8	R70, R71, R316, R317, R338, R339, R360, R361	15 Ohm	PANASONIC	ERJ-3EKF15R0V	RES 15 OHM 1/10W 1% 0603 SMD
4	R77, R152, R373, R374	56K	PANASONIC	ERJ-3EKF5602V	RES 56.0K OHM 1/10W 1% 0603 SMD
3	R78, R375, R400	56.2K Ohm	PANASONIC	ERJ-3EKF5622V	RES 56.2K OHM 1/10W 1% 0603 SMD
8	R82, R83, R308, R309, R330, R331, R352, R353	250 ohm	VISHAY	PLT0603Z2500AST5	RES 250 OHM 0.05% 5PPM 0603 SMD
30	R84, R102, R108, R109, R110, R112, R154, R155, R165, R166, R167, R168, R180, R182, R183, R184, R185, R188, R297, R298, R299, R300, R301, R302, R303, R310, R332, R354, R378, R379	0 ohm	PANASONIC	ERJ-3GEY0R00V	DNI; RESISTOR,SMT,0603,0 OHM,5%,ZERO OHM JUMPER
1	T15	TC4-1WG2+	Mini-Circuits	TC4-1WG2+	
16	T26, T27, T28, T29, T30, T31, T32, T33, T34, T35, T36, T37, T38, T39, T40, T41	ADT4-1WT	Mini-Circuits	ADT4-1WT+	
16	TP2, TP9, TP19, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35	T POINT R	Keystone Electronics	5001	
1	U1	ADS5296	Texas Instruments	ADS5296IRGC	TI Supplied Device
2	U10, U30	TPS73201-SOT23	Texas Instruments	TPS73201DBVR	IC LDO REG 250MA ADJ-V SOT23-5
2	U11, U12	TPS77533D	Texas Instruments	TPS77533D	IC 3.3V 500MA LDO REG 8-SOIC
4	U17, U27, U28, U29	THS770006	Texas Instruments	THS770006IRGER	IC AMP DIFF ADC DVR 16BIT 24VQFN
1	U2	80 MHZ	ECS INC	ECS-3953M-800-BN	OSCILLATOR, 80 MHZ, 4-PIN
1	U21	CDCLVP1102	Texas Instruments	CDCLVP1102RGTT	IC CLK BUFF 1:2 LVPECL SGL 16QFN
1	U31	2.7 V TO 5.5 V	TEXAS INSTRUMENTS	OPA4353EA	IC OPAMP GP R-R 44MHZ 16QSOP
1	U6	FT245RL	FTDI Chip	FT245RL	IC USB TO PARALLEL FIFO 28-SSOP
18	Z_SH-H3, Z_SH-H4, Z_SH-H5, Z_SH-H6, Z_SH-H7, Z_SH-H8, Z_SH-H9, Z_SH-H10, Z_SH- H11, Z_SH-H14, Z_SH-H16, Z_SH-H17, Z_SH-H18, Z_SH-H19, Z_SH-H20, Z_SH-H21, Z_SH-H22, Z_SH-H23	SHUNT-HEADER	Keltron	MJ-5.97-G-F1 or equivalent	SHUNT FOR HEADER

ADS5296 EVM Layout

www.ti.com

8 ADS5296 EVM Layout

Figure 88 through Figure 93 illustrate the PCB layouts for the EVM.



Figure 88. ADS5296 EVM Top Layer Assembly Drawing – Top View

Texas Instruments



1



Figure 89. ADS5296 EVM Bottom Layer Assembly Drawing – Bottom View





Figure 90. ADS5296 EVM Top Side





Figure 91. ADS5296 EVM Ground Plane





Figure 92. ADS5296 EVM Signal Plane





Figure 93. ADS5296 EVM Bottom Side

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications			
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive		
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications		
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers		
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps		
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy		
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial		
Interface	interface.ti.com	Medical	www.ti.com/medical		
Logic	logic.ti.com	Security	www.ti.com/security		
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense		
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video		
RFID	www.ti-rfid.com				
OMAP Applications Processors	www.ti.com/omap	TI E2E Community	e2e.ti.com		
Wireless Connectivity	www.ti.com/wirelessconnectivity				

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2015, Texas Instruments Incorporated