CMOS 8-Bit Microcontroller

TMP86FM48UG/FG

The TMP86FM48 is the high-speed, high-performance and low power consumption 8-bit microcomputer, including FLASH, RAM, multi-function timer/counter, serial interface (UART, SIO, I²C), a 10-bit AD converter and two clock generators on chip.

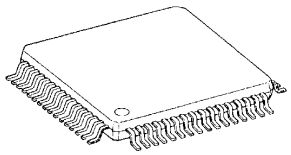
Product No.	FLASH (Program area)	FLASH (Data area)	RAM	Package	Emulation Chip
TMP86FM48UG	32256 × 8 bits	512 × 8 bits	2.0 K × 8 bits	P-LQFP64-1010-0.50E	*TMP86C948XB
TMP86FM48FG				P-QFP64-1414-0.80C	

*: Under development

Features

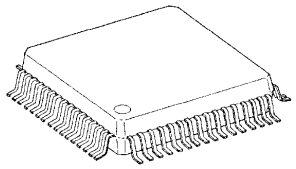
- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.25 μs (at 16 MHz)
  122 μs (at 32.768 kHz)
- 132 types and 731 basic instructions
- 20 interrupt sources (External: 5, Internal: 15)
- Input/output ports (54 pins)
- 16-bit timer counter: 2 ch
  - Timer, Event counter,
    Pulse width measurement, External trigger timer,
    Window, PPG output modes
- 8-bit timer counter: 2 ch
  - Timer, Event counter, PWM output,
    Programmable divider output, Capture modes
- Time base timer
- Divider output function

P-LQFP64-1010-0.50E



TMP86FM48UG

P-QFP64-1414-0.80C



TMP86FM48FG

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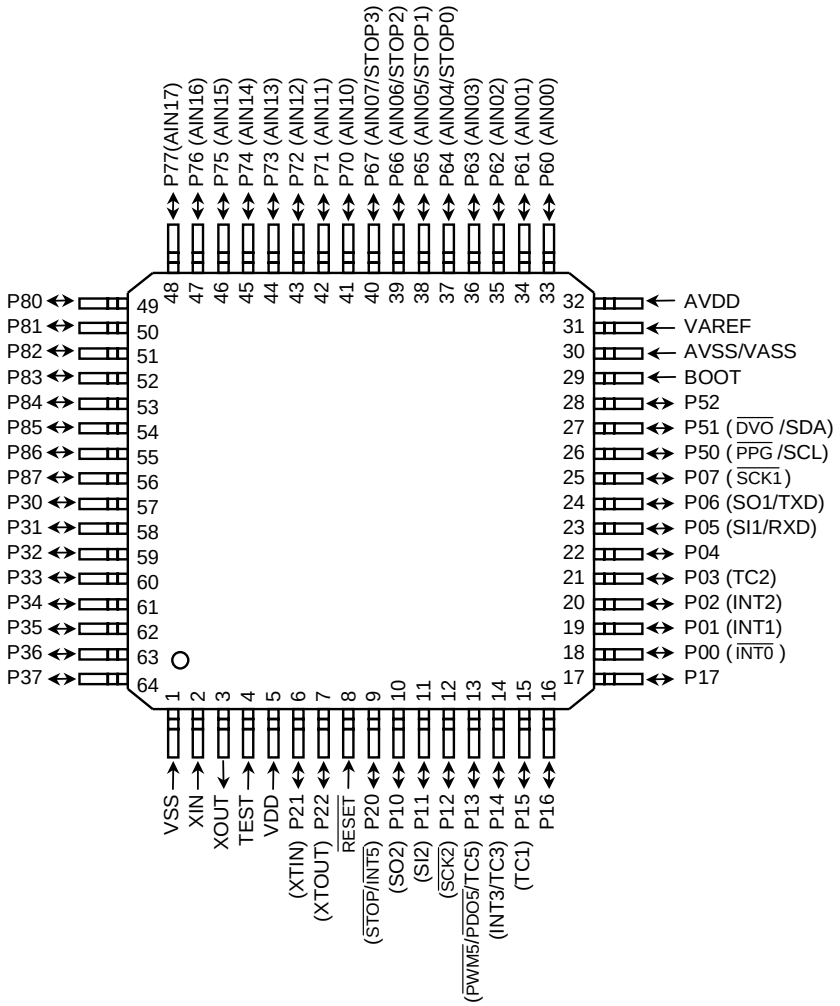
Purchase of TOSHIBA I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

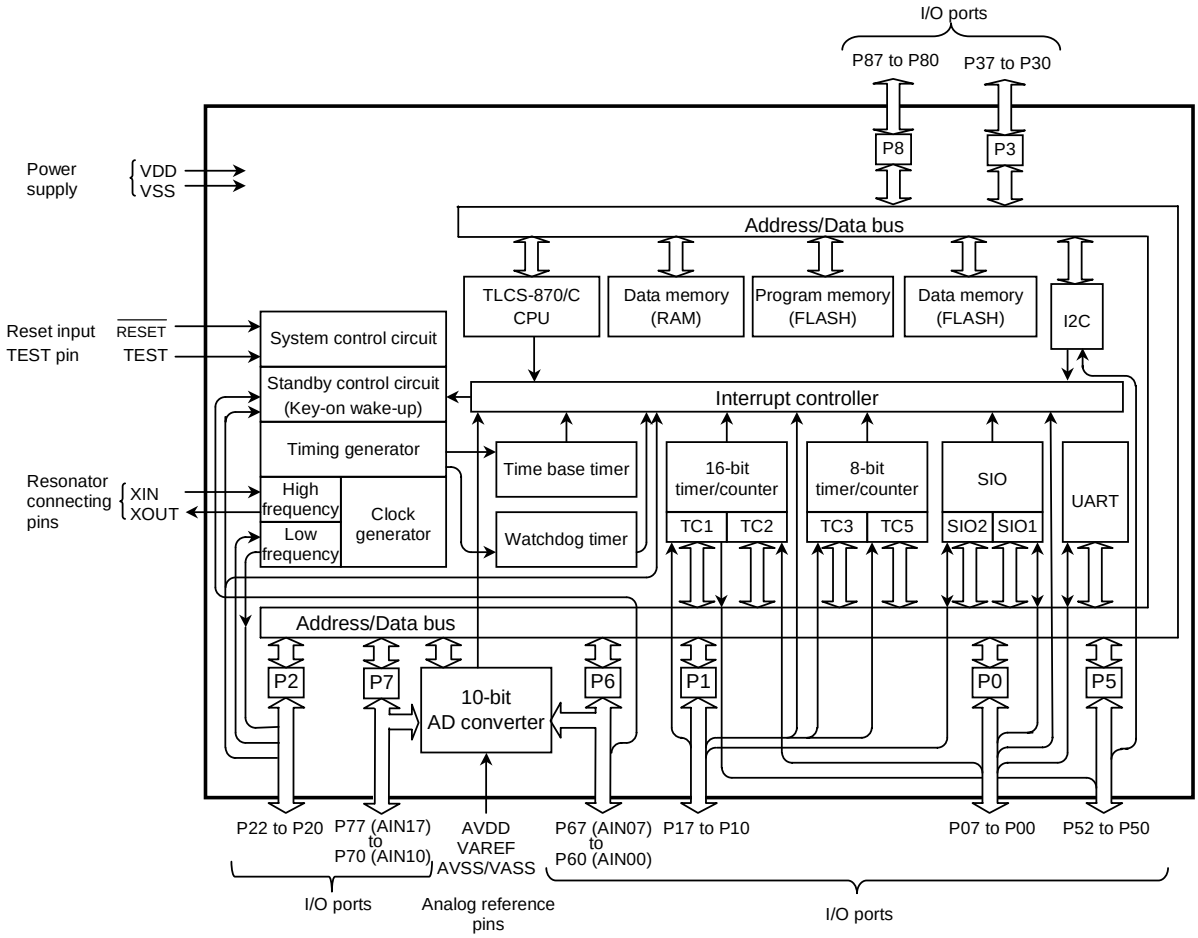
- Watchdog timer
  - Interrupt source/internal reset generate (Programmable)
- Serial interface
  - UART/SIO: 1ch
  - SIO: 1ch
  - I^2C bus: 1ch
- 10-bit successive approximation type AD converter
  - Analog input: 16 ch
- Four Key-on wake-up pins
- Dual clock operation
  - Single/dual-clock mode
- Nine power saving operating modes
  - STOP mode: Oscillation stops. Battery/capacitor back-up. Port output hold/High-impedance.
  - SLOW 1, 2 mode: Low-power consumption operation using low-frequency clock (32.768 kHz)
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by falling edge of TBTCR<TBTCK> setting.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interruputs.
  - IDLE 2 mode: CPU stops, and peripherals operate using high and low-frequency clock. Release by interruputs.
  - SLEEP 0 mode: CPU stops, and peripherals operate using low-frequency clock of time-base-timer. Release by falling edge of TBTCR<TBTCK> setting.
  - SLEEP 1 mode: CPU stops, and peripherals operate using low-frequency clock. Release by interrupts.
  - SLEEP 2 mode: CPU stops, and peripherals operate using high- and low-frequency clock. Release by interrupts.
- Wide operating voltage: 1.8 to 3.6 V at 8 MHz/32.768 kHz
  2.7 to 3.6 V at 16 MHz/32.768 kHz

Pin Assignments (Top view)

P-LQFP64-1010-0.50E
P-QFP64-1414-0.80C



Block Diagram



Pin Functions (1/2)

Pin Name	Input/Output	Functions		
P07 ($\overline{SCK1}$)	I/O (I/O)	8-bit input/output port with latch. When used as a serial interface output or UART output, respective output latch (P0DR) should be set to “1”. When used as an input port, an serial interface input, UART input, timer counter input or an external interrupt input, respective output control (P0OUTCR) should be cleared to “0” after setting P0DR to “1”.	Serial clock input/output 1	
P06 (TXD, SO1)	I/O (Output)		UART data output, Serial data output 1	
P05 (RXD, SI1)	I/O (Input)		UART data input, Serial data input 1	
P04	I/O			
P03 (TC2)	I/O (Input)		Timer counter 2 input	
P02 (INT2)	I/O (Input)		External interrupt 2 input	
P01 (INT1)	I/O (Input)		External interrupt 1 input	
P00 ($\overline{INT0}$)	I/O (Input)		External interrupt 0 input	
P17	I/O	8-bit input/output port with latch. When used as a timer/counter output or serial interface output, respective output latch (P1DR) should be set to “1”. When used as an input port, a timer counter input, an external interrupt input or serial interface input, respective output control (P1OUTCR) should be cleared to “0” after setting P1DR to “1”.		
P16	I/O			
P15 (TC1)	I/O (Input)		Timer counter 1 input	
P14 (TC3,INT3)	I/O (Input)		Timer counter 3 input, External interrupt 3 input	
P13 ($\overline{PWM5}$, $\overline{PDO5}$, TC5)	I/O (I/O)		PWM5 output, PDO5 output, Timer/counter 5 input	
P12 ($\overline{SCK2}$)	I/O (I/O)		Serial clock input/output 2	
P11 (SI2)	I/O (Input)		Serial data input 2	
P10 (SO2)	I/O (Output)		Serial data output 2	
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port or an external interrupt input, respective output control (P2OUTCR) should be cleared to “0” after setting output latch (P2DR) to “1”.	Resonator connecting pins (32.768 kHz) For inputting external clock, XTIN is used and XTOUT is opened.	
P21 (XTIN)	I/O (Input)			
P20 ($\overline{INT5}$, $\overline{STOP}$)	I/O (Input)		External interrupt input 5 or STOP mode release signal input	
P37 to P30	I/O	8-bit input/output port with latch (N-ch high-current output). When used as an input port, respective output control (P3OUTCR) should be cleared to “0” after setting output latch (P3DR) to “1”.		
P52	I/O	3-bit input/output port with latch (N-ch high-current output). When used as an input port or I^2C bus interface input/output, respective output control (P5OUTCR) should be cleared to “0” after setting output latch (P5DR) to “1”. When used as a PPG output or divider output, respective P5DR should be set to “1”.		
P51 ($\overline{DVO}$, SDA)	I/O (Output,I/O)		Divider Output/I^2C bus serial data input/output	
P50 ($\overline{PPG}$, SCL)	I/O (Output,I/O)		PPG Output/I^2C bus serial clock input/output	
P67 (AIN07, STOP3)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as an input port, respective input/output control (P6CR1) should be cleared to “0” after setting input control (P6CR2) to “1”. When used as an analog input or key on wake up input, respective P6CR1 should be cleared to “0” after clearing P6CR2 to “0”. When used as a key on wake up input, STOPCR<STOPiEN > should be set to “1”. (i = 0 to 3)	STOP 3 input	AD converter analog inputs
P66 (AIN06, STOP2)	I/O (Input)		STOP 2 input	
P65 (AIN05, STOP1)	I/O (Input)		STOP 1 input	
P64 (AIN04, STOP0)	I/O (Input)		STOP 0 input	
P63 (AIN03)	I/O (Input)			
P62 (AIN02)	I/O (Input)			
P61 (AIN01)	I/O (Input)			
P60 (AIN00)	I/O (Input)			

Pin Functions (2/2)

Pin Name	Input/Output	Functions	Pin Name
P77 (AIN17)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as an input port, respective input/output control (P7CR1) should be cleared to “0” after setting input control (P7CR2) to “1”. When used as an analog input, respective P7CR1 should be cleared to “0” after clearing P7CR2 to “0”.	AD converter analog inputs
P76 (AIN16)	I/O (Input)		
P75 (AIN15)	I/O (Input)		
P74 (AIN14)	I/O (Input)		
P73 (AIN13)	I/O (Input)		
P72 (AIN12)	I/O (Input)		
P71 (AIN11)	I/O (Input)		
P70 (AIN10)	I/O (Input)		
P87 to P80	I/O	8-bit input/output port with latch (N-ch high-current output). When used as an input port, respective output control (P8OUTCR) should be cleared to “0” after setting output latch (P8DR) to “1”.	
XIN, XOUT	Input Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	Input	Reset signal input	
TEST	Input	Test pin for out-going test. Be fixed to low.	
BOOT	Input	Serial prom mode control input. When writing to FLASH memory, BOOT pin should be fixed to high level.	
VDD, VSS	Power Supply	Power supply for operation	
VAREF		Analog reference voltage for AD conversion	
AVDD		AD circuit power supply	
AVSS/VASS		AD circuit power supply/Analog reference GND for AD conversion	

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

1.1 Memory Address Map

The TMP86FM48 memory consists of 5 blocks: FLASH memory, BOOT ROM, RAM, DBR (Data buffer register) and SFR (Special function register). They are all mapped in 64-Kbyte address space. Figure 1.1.1 shows the TMP86FM48 memory address map. The general-purpose registers are not assigned to the RAM address space.

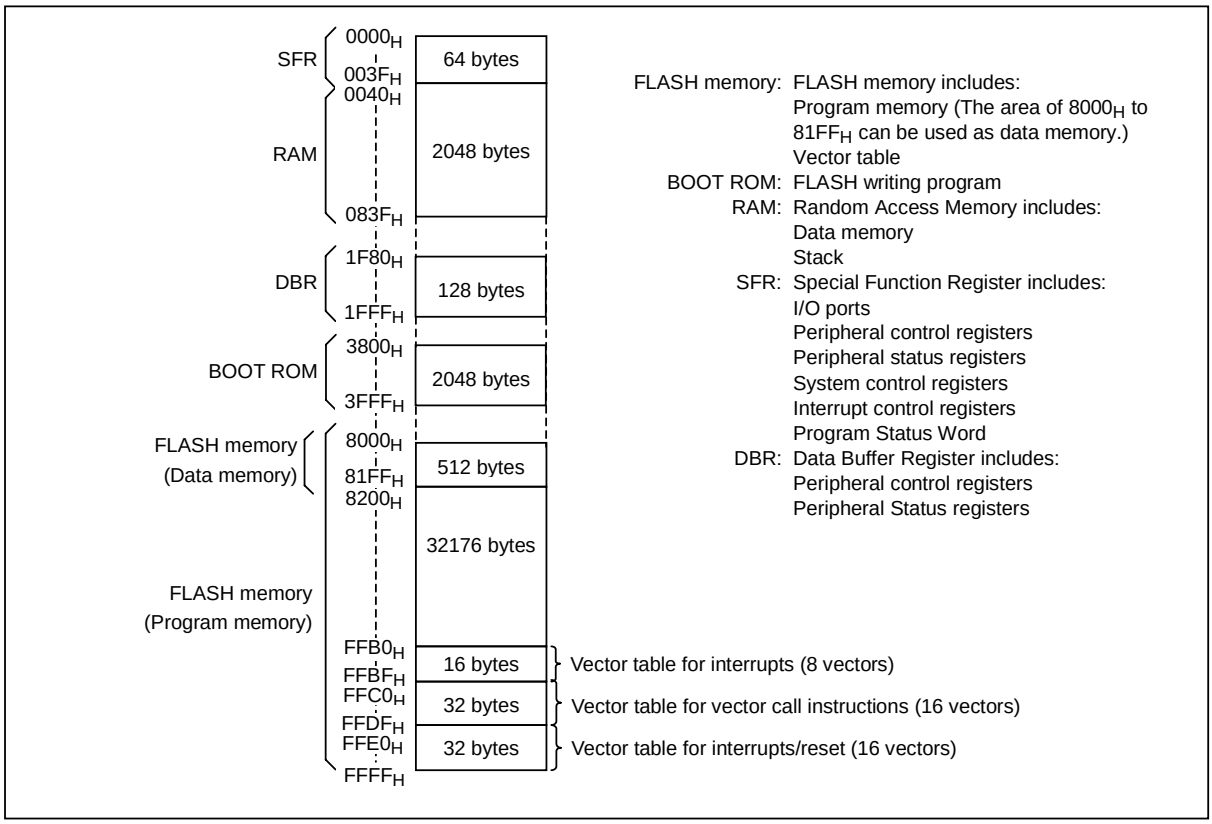


Figure 1.1.1 Memory Address Maps

1.2 Program Memory (FLASH)

The TMP86FM48 has a 32 K × 8 bits (Address 8000_H to $FFFF_H$) of program memory (FLASH). The area of 8000H to 81FFH can be used as a 512 × 8 bits data memory of FLASH.

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply voltage	V_{DD}		−0.3 to 4.0	V
Input voltage	V_{IN}		−0.3 to V_{DD} + 0.3	
Output voltage	V_{OUT1}		−0.3 to V_{DD} + 0.3	
Output current (Per 1 pin)	I_{OUT1}	P0, P1, P20, P3, P5, P6, P7, P8 ports	−2	mA
	I_{OUT2}	P0, P1, P2, P4, P6, P7, P8 ports	2	
	I_{OUT3}	P3, P5 ports	10	
Output current (Total)	ΣI_{OUT1}	P0, P1, P20, P3, P5, P6, P7, P8 ports	−80	
	ΣI_{OUT2}	P0, P1, P2, P4, P6, P7, P8 ports	80	
	ΣI_{OUT3}	P3, P5 ports	30	
Power dissipation [Topr = 85°C]	PD		350	mW
Soldering temperature (Time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		−55 to 125	
Operating temperature	Topr		−40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition-1 (MCU mode) (V_{SS} = 0 V, Topr = −40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 mode	2.7	3.6	V
				IDLE0, 1, 2 mode			
			fc = 8 MHz (In case of connecting the resonator)	NORMAL1, 2 mode	1.8		
				IDLE0, 1, 2 mode			
			fc = 4.2 MHz (In case of external clock input)	NORMAL1, 2 mode			
				IDLE0, 1, 2 mode			
			fs = 32.768 kHz	SLOW1, 2 mode	1.8		
				SLEEP0, 1, 2 mode			
				STOP mode			
Input high level	V_{IH1}	Except Hysteresis input	$V_{DD} \geq 2.7$ V		$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 2.7$ V		$V_{DD} \times 0.90$		
Input low level	V_{IL1}	Except Hysteresis input	$V_{DD} \geq 2.7$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 2.7$ V			$V_{DD} \times 0.10$	
Clock frequency (In case of connecting the resonator)	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	8.0	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz
Clock frequency (In case of external clock input)	fc	XIN, XOUT	V_{DD} = 1.8 to 3.6 V		1.0	4.2	MHz
			V_{DD} = 2.7 to 3.6 V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 1.8 to 3.6 V		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (Supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Recommended Operating Condition-2 (Serial PROM mode) (V_{SS} = 0 V, Topr = 25°C ± 5°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	VDD		2 MHz ≤ fc ≤16 MHz	2.7	3.6	V
Clock frequency	fc	XIN, XOUT	VDD = 2.7 to 3.6 V	2.0	16.0	MHz

Note: The operating temperature area of serial PROM mode is 25°C ± 5°C and the operating area of high frequency of serial PROM mode is different from MCU mode.

DC Characteristics (V_{SS} = 0 V, Topr = −40 to 85°C)

Parameter	Symbol	Pins	Condition		Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input	V_{DD} = 3.3 V		–	0.4	–	V
Input current	I_{IN1}	TEST	V_{DD} = 3.6 V, V_{IN} = 0 V		–	–	−5	μA
	I_{IN2}	Sink open drain, Tri-state	V_{DD} = 3.6 V, V_{IN} = 3.6 V/0 V		–	–	±5	
	I_{IN3}	$\overline{\text{RESET}}$	V_{DD} = 3.6 V, V_{IN} = 3.6 V		–	–	+5	
Input resistance	R_{IN1}	TEST pull down	V_{DD} = 3.6 V, V_{IN} = 3.6 V		–	70	–	kΩ
	R_{IN2}	BOOT pull down	V_{DD} = 3.6 V, V_{IN} = 3.6 V		–	70	–	
	R_{IN3}	$\overline{\text{RESET}}$ pull up P21, P22 ports	V_{DD} = 3.6 V, V_{IN} = 0 V		100	220	450	
High frequency feedback resistor	R_{FB}	XOUT	V_{DD} = 3.6 V		–	3	–	MΩ
Low frequency feedback resistor	R_{FBT}	XTOUT	V_{DD} = 3.6 V		–	20	–	
Output leakage current	I_{LO}	Sink open drain, Tri-state	V_{DD} = 3.6 V V_{OUT} = 3.4V/0.2 V		–	–	±10	μA
Output high voltage	V_{OH}	CMOS, Tri-state	V_{DD} = 3.6 V, I_{OH} = −0.6 mA		3.2	–	–	V
Output low voltage	V_{OL}	Except XOUT, P3 and P5 ports	V_{DD} = 3.6 V, I_{OL} = 0.9 mA		–	–	0.4	
Output low current	I_{OL}	P3, P5 ports	V_{DD} = 3.6 V, V_{OL} = 1.0 V		–	6	–	mA
Supply current in NORMAL 1, 2 mode	I_{DD}	Fetch area: Flash area	V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V fc = 16 MHz fs = 32.768 kHz	MNP = "1"	–	5.0	6.0	mA
		Fetch area: RAM area		MNP = "0"	–	3.5	4.8	
Supply current in IDLE 0, 1, 2 mode				MNP•ATP = "1"	–	3.5	4.5	
				MNP•ATP = "0"	–	2.5	3.7	
Supply current in SLOW 1 mode		Fetch area: Flash area	V_{DD} = 3.0 V V_{IN} = 2.8 V/0.2 V fs = 32.768 kHz	MNP = "1"	–	800	1400	μA
		Fetch area: RAM area		MNP = "0"	–	6	20	
Supply current in SLEEP 1 mode				MNP•ATP = "1"	–	800	1400	
				MNP•ATP = "0"	–	5	18	
Supply current in SLEEP 0 mode				MNP•ATP = "1"	–	800	1400	
				MNP•ATP = "0"	–	5	18	
Supply current in STOP mode			V_{DD} = 3.6 V V_{IN} = 3.4 V/0.2 V		–	0.5	10	

Note 1: Typical values show those at Topr = 25°C.

Note 2: Input current (I_{IN1}, I_{IN2}): The current through pull-up or pull-down resistor is not included.

Note 3: I_{DD} does not include I_{REF} current.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent to IDLE0, IDLE1, IDLE2.

Note 5: MNP (MNPWDW) shows bit0 in EEPCR register and ATP (ATPWDW) shows bit1 in EEPCR register.

Note 6: "Fetch" means reading operation of FLASH data as an instruction by CPU.

AD Conversion Characteristics (V_{SS} = 0.0 V, 2.7 V ≤ V_{DD} ≤ 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 3.6 V V_{SS} = 0.0 V	–	0.35	0.61	mA
Non linearity error		V_{DD} = A_{VDD} = 2.7 V V_{SS} = 0.0 V V_{AREF} = 2.7 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

(V_{SS} = 0.0 V, 2.0 V ≤ V_{DD} < 2.7 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 0.6	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		2.0	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 2.0V V_{SS} = 0.0 V	–	0.20	0.34	mA
Non linearity error		V_{DD} = A_{VDD} = 2.0 V V_{SS} = 0.0 V V_{AREF} = 2.0 V	–	–	±4	LSB
Zero point error			–	–	±4	
Full scale error			–	–	±4	
Total error			–	–	±4	

(V_{SS} = 0.0 V, 1.8 V ≤ V_{DD} < 2.0 V, Topr = –10 to 85°C) (Note 5)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} – 0.1	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	ΔV_{AREF}		1.8	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 1.8 V V_{SS} = 0.0 V	–	0.18	0.31	mA
Non linearity error		V_{DD} = A_{VDD} = 1.8 V V_{SS} = 0.0 V V_{AREF} = 1.8 V	–	–	±4	LSB
Zero point error			–	–	±4	
Full scale error			–	–	±4	
Total error			–	–	±4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is different in recommended value by power supply voltage.
About conversion time, please refer to “2.15.2 Register configration”.

Note 3: Please use input voltage to AIN input Pin in limit of VAREF – VSS.
When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.

Note 4: Analog Reference Voltage Range: ΔVAREF = VAREF – VSS

Note 5: When AD is used with VDD < 2.0 V, the guaranteed temperature range varies with the operating voltage.

Note 6: When AD converter is not used, fix the AVDD pin and VAREFpin on the V_{DD} level.

AC Characteristics (V_{SS} = 0 V, V_{DD} = 2.7 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.25	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High Level clock pulse width	twcH	For external clock operation (XIN input), fc = 16 MHz	–	31.25	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input), fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

(V_{SS} = 0 V, V_{DD} = 1.8 to 3.6 V, Topr = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 mode	0.5	–	4	μs
		IDLE1, 2 mode				
		SLOW1, 2 mode	117.6	–	133.3	
		SLEEP1, 2 mode				
High level clock pulse width	twcH	For external clock operation (XIN input), fc = 4.2 MHz	–	119.04	–	ns
Low level clock pulse width	twcL					
High level clock pulse width	twcH	For external clock operation (XTIN input), fs = 32.768 kHz	–	15.26	–	μs
Low level clock pulse width	twcL					

Flash Characteristics (V_{SS} = 0 V)

Parameter	Condition	Min	Typ.	Max	Unit
Number of guaranteed writes (page writing) to Flash memory in serial PROM mode	V_{DD} = 2.7 to 3.6 V, 2 MHz ≤ fc ≤ 16 MHz (Topr = 25°C ± 5°C)	–	–	10^5	Times
Number of guaranteed writes (page writing) to Flash data memory in MCU mode	V_{DD} = 1.8 to 3.6 V at fc = 8 MHz V_{DD} = 2.7 to 3.6 V at fc = 16 MHz (Topr = –40 to 85°C)	–	–	10^5	
Writing time to Flash data memory for one page (64 bytes) in MCU mode		–	4	6	ms

Recommended Oscillating Conditions

Note 1: An electrical shield by metal shield plate on the surface of IC package is recommended in order to protect the device from the high electric field stress applied from CRT (Cathodic Ray Tube) for continuous reliable operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following
http://www.murata.co.jp/search/index.html