SN65MLVD048
SLLS903A – DECEMBER 2009 – REVISED MARCH 2024

SN65MLVD048 Quad Channel M-LVDS Receivers

1 Features

- Low-voltage differential 30Ω to 55Ω line receivers for signaling rates[1] up to 250Mbps; Clock Frequencies up to 125MHz
- Type-1 receiver incorporates 25mV of input threshold hysteresis
- Type-2 receiver provides 100mV offset threshold to detect open-circuit and idle-bus conditions
- Wide receiver input common-mode voltage range, –1V to 3.4V, allows 2V of ground noise
- Meets or exceeds the M-LVDS standard TIA/EIA-899 for multipoint topology
- High input impedance when $V_{CC} \leq 1.5V$
- Enhanced ESD Protection: 7kV HBM on all pins
- 48-Pin 7 X 7 QFN (RGZ)

2 Applications

- Parallel multipoint data and clock transmission via backplanes and cables
- Cellular base stations
- Central office switches
- Network switches and routers

3 Description

The SN65MLVD048 is a quad-channel M-LVDS receiver. This device is designed in full compliance with the TIA/EIA-899 (M-LVDS) standard, which is optimized to operate at signaling rates up to 250Mbps. Each receiver channel is controlled by a receive enable ($\overline{RE}$). When $\overline{RE}$ = low, the corresponding channel is enabled; when $\overline{RE}$ = high, the corresponding channel is disabled.

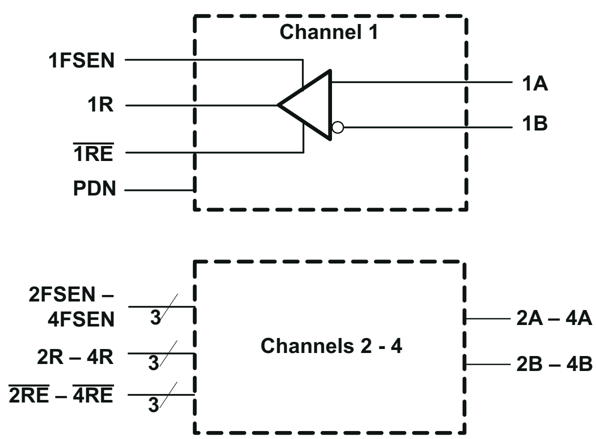
The M-LVDS standard defines two types of receivers, designated as Type-1 and Type-2. Type-1 receivers have thresholds centered about zero with 25mV of hysteresis to prevent output oscillations with loss of input; Type-2 receivers implement a failsafe by using an offset threshold. Receiver outputs are slew rate controlled to reduce EMI and crosstalk effects associated with large current surges.

The devices are characterized for operation from –40°C to 85°C.

Package Information

PART NUMBER	PACKAGE[(1)]	PACKAGE SIZE[(2)]
SN65MLVD048	VQFN (RGZ, 48)	7mm x 7mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

[1] The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

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4 Pin Configuration and Functions

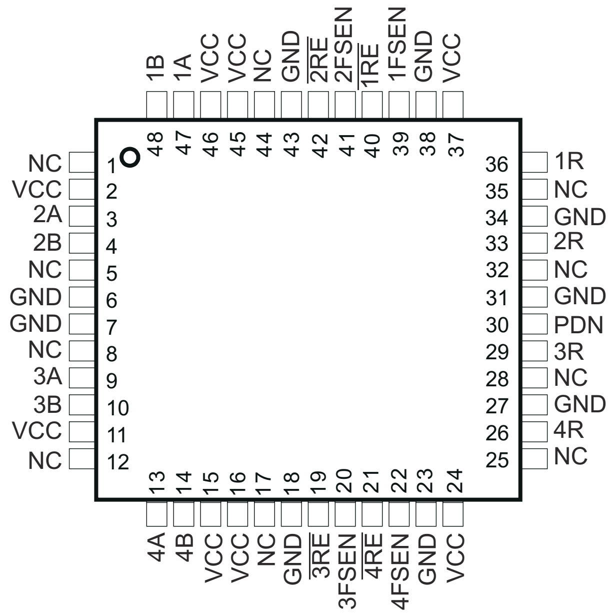


Figure 4-1. RGZ Package (Top View)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
1R—4R	36, 33, 29, 26	O	Data output from receivers
1A–4A	47, 3, 9, 13	I/O	M-LVDS bus non-inverting input/output
1B–4B	48, 4, 10, 14	I/O	M-LVDS bus inverting input/output
GND	6, 7, 18, 23, 27, 31, 34, 38, 43	I	Circuit ground. **ALL GND pins must be connected to ground.**
V_{CC}	2, 11, 15, 16, 24, 37, 45, 46	I	Supply voltage. **ALL VCC pins must be connected to supply.**
$\overline{1RE}$– $\overline{4RE}$	40, 42, 19, 21	I	Receiver enable, active low, enables individual receivers. When this pin is left floating, internally this pin will be pulled to logic HIGH.
1FSEN–4FSEN	39, 41, 20, 22	I	Failsafe enable pin. When this pin is left floating, internally this pin will be pulled to logic HIGH. This pin enables the Type 2 receiver for the respective channel. xFSEN = L → Type 1 receiver inputs xFSEN = H → Type 2 receiver inputs
PDN	30		Power Down pin. When this pin is left floating, internally this pin will be pulled to logic LOW. When PDN is HIGH, the device is powered up. When PDN is LOW, the device overrides all other control and powers down. All outputs are Hi-Z
NC	1, 5, 8, 12, 17, 25, 28, 32, 35		Not Connected
NC	44		Not Connected. Internal TI Test pin. **This pin must be left unconnected.**
PowerPAD™	–		Connected to GND

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range[(2)]		–0.5		4	V
	Input voltage range	$\overline{RE}$, FSEN	–0.5		4	V
		A or B	–1.8		4	V
	Output voltage range	R	–0.3		4	V
P_D	$\overline{RE}$ at 0V, C_L = 15pF, V_{ID} = 400mV, 125MHz				339	mW
T_{stg}	Storage Temperature		–65		150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±7000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	GND		0.8	V
V_A or V_B	Voltage at any bus terminal	–1.4		3.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	0.05		V_{CC}	V
V_{IC}	Differential common-mode input voltage	–1		3.4	V
R_L	Differential load resistance	30	50		Ω
$1/t_{UI}$	Signaling rate			250	Mbps
T_A	Operating free-air temperature	–40		85	°C

5.4 Package Dissipation Ratings

PACKAGE[(1)]	PCB TYPE	T_A ≤ 25°C POWER RATING	DERATING FACTOR[(2)] ABOVE T_A = 25°C	T_A = 85°C POWER RATING
48-Pin QFN (RGZ)	Low-K	1298 mW	12.98 mW/°C	519 mW
	High-K	3448 mW	34.48 mW/°C	1379 mW

(1) The thermal dissipations are in the consideration of soldering down the powerPAD without via on each type of boards.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.5 Thermal Information

THERMAL METRIC[1]		RGZ 48-Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.6 Device Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current	$\overline{RE}$ at 0V for all channels C_L = 15pF, V_{ID} = 400mV, 125MHz		86	94	mA
	Power down	PDN = L		0.75	1.5	mA

(1) All typical values are at 25°C and with a 3.3V supply voltage.

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	Type 1	See Table 6-1 and Table 6-2			35	mV
		Type 2				135	
V_{IT-}	Negative-going differential input voltage threshold	Type 1		–35			mV
		Type 2		65			
V_{HYS}	Differential input voltage hysteresis (V_{IT+} – V_{IT-})	Type 1			25		mV
		Type 2			0		
V_{OH}	High-level output voltage		I_{OH} = –8mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8mA			0.4	V
I_{IH}	High-level input current		V_{IH} = 2V to V_{CC}	–10			µA
I_{IL}	Low-level input current		V_{IL} = GND to 0.8V	–10			µA
I_{OZ}	High-impedance output current		V_O = 0V or V_{CC}	–10		15	µA
I_A or I_B	Receiver input current		One input (V_A or V_B) = –1.4V or 3.8V, Other input = 1.2V	–20		20	µA
I_{AB}	Receiver differential input current (I_A – I_B)		V_A = V_B = –1.4V or 3.8V	–4		4	µA
$I_{A(OFF)}$ or $I_{B(OFF)}$	Receiver input current		One input (V_A or V_B) = –1.4V or 3.8V, Other input = 1.2V, V_{CC} = GND or 1.5V	–32		32	µA
$I_{AB(OFF)}$	Receiver power-off differential input current (I_A – I_B)		V_A = V_B = –1.4V or 3.8V, V_{CC} = GND or 1.5V	–4		4	µA
C_A or C_B	Input capacitance		V_I = 0.4sin(30E6πt) + 0.5V,[2] Other input at 1.2V		5		pF
C_{AB}	Differential input capacitance		V_{AB} = 0.4sin(30E6πt) + 0.5V[2]			3	pF
$C_{A/B}$	Input capacitance balance, (C_A/C_B)			0.99		1.01	

(1) All typical values are at 25°C and with a 3.3V supply voltage.
(2) HP4194A impedance analyzer (or equivalent)

5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 15pF, See Figure 6-2	2		6	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2		6	ns
t_r	Output signal rise time			1		2.3	
t_f	Output signal fall time			1		2.3	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	Type 1			35	270	ps
		Type 2			150	460	
$t_{sk(pp)}$	Part-to-part skew					800	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)[(2)]		All channels switching, 125MHz clock input[(3)], See Figure 6-4			6	ps
$t_{jit(c-c)}$	Cycle-to-cycle jitter, rms[(2)]					13	ps
$t_{jit(det)}$	Deterministic jitter[(2)]	Type 1	All channels switching, 250Mbps 2^{15}-1 PRBS input[(3)], See Figure 6-4			800	ps
		Type 2				945	ps
$t_{jit(ran)}$	Random jitter[(2)]	Type 1				9	ps
		Type 2				8	ps
t_{PZH}	Enable time, high-impedance-to-high-level output		C_L = 15pF, See Figure 6-3			15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output		C_L = 15pF, See Figure 6-3			15	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output		C_L = 15pF, See Figure 6-3			10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output		C_L = 15pF, See Figure 6-3			10	ns

(1) All typical values are at 25°C and with a 3.3V supply voltage.
(2) Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
(3) $t_r = t_f$ = 0.5ns (10% to 90%)

5.9 Typical Characteristics

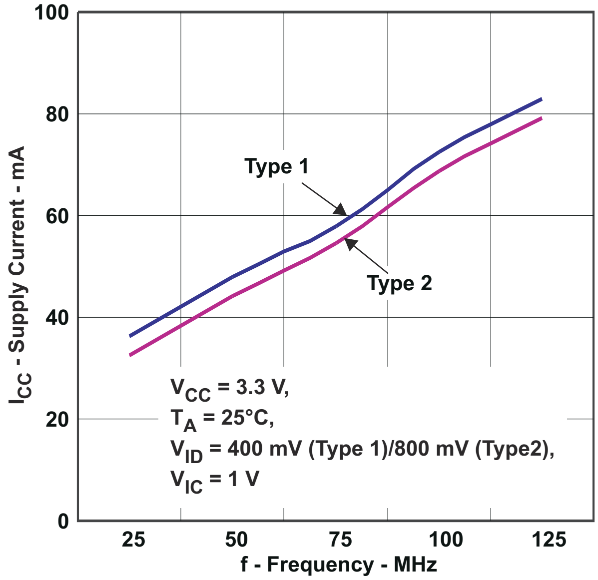


Figure 5-1. Supply Current vs Frequency

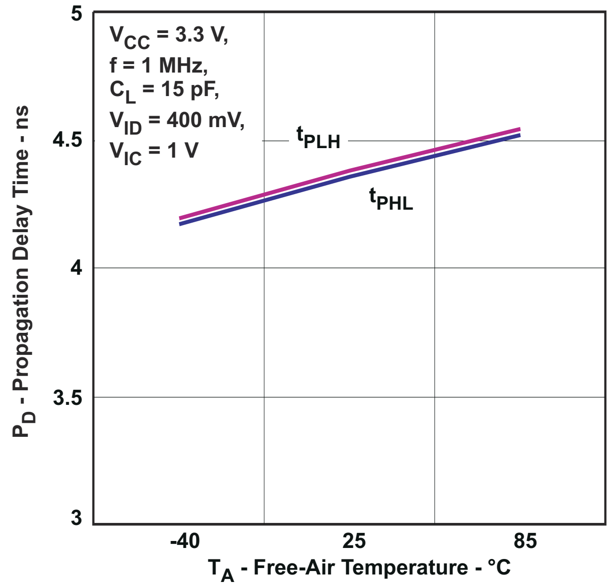


Figure 5-2. Receiver (Type-1) Propagation Delay Time vs Free-Air Temperature

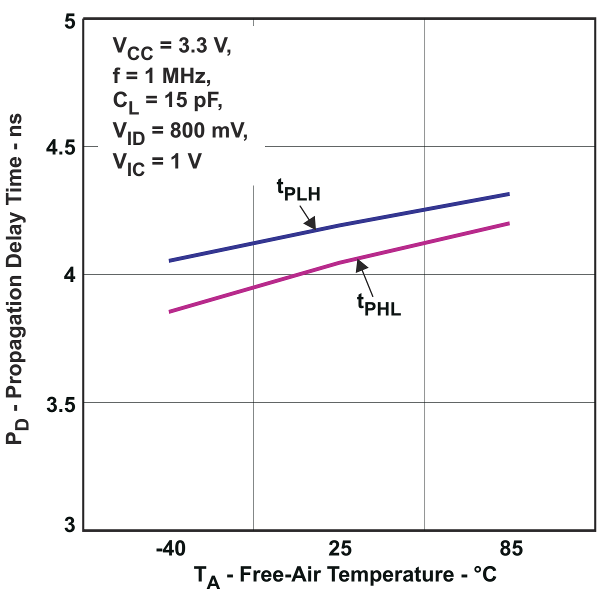


Figure 5-3. Receiver (Type-2) Propagation Delay Time vs Free-Air Temperature

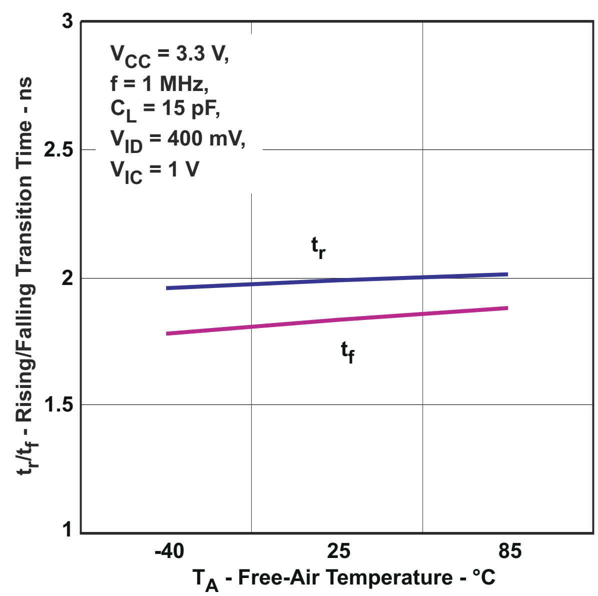


Figure 5-4. Receiver (Type-1) Transition Time vs Free-Air Temperature

5.9 Typical Characteristics (continued)

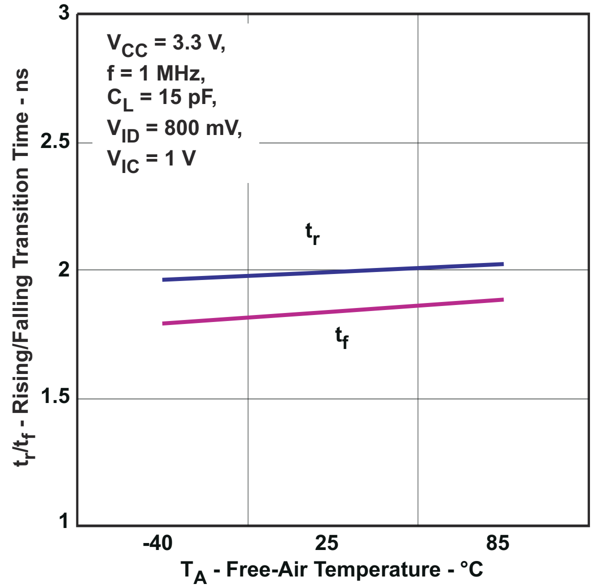


Figure 5-5. Receiver (Type-2) Transition Time vs Free-Air Temperature

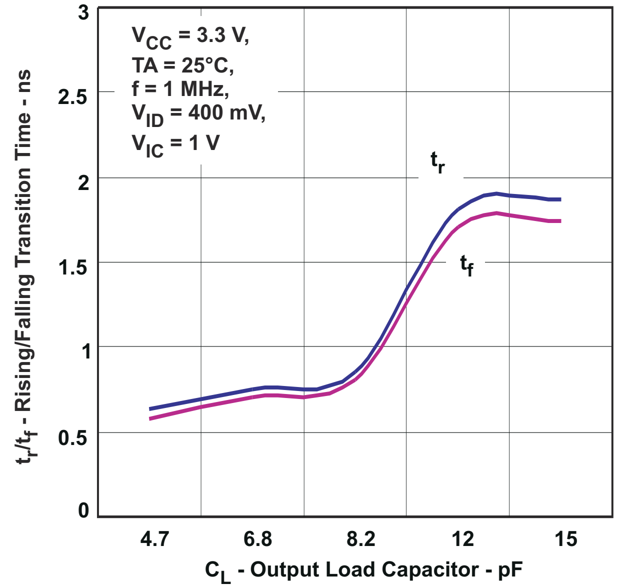


Figure 5-6. Receiver (Type-1) Transition Time vs Output Load Capacitor

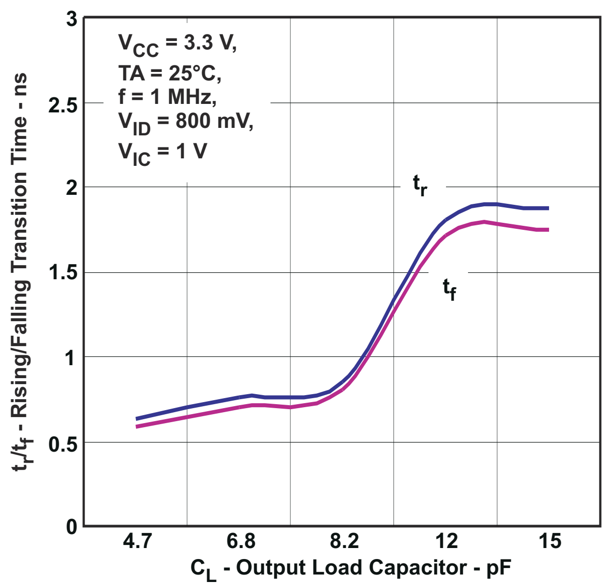


Figure 5-7. Receiver (Type-2) Transition Time vs Output Load Capacitor

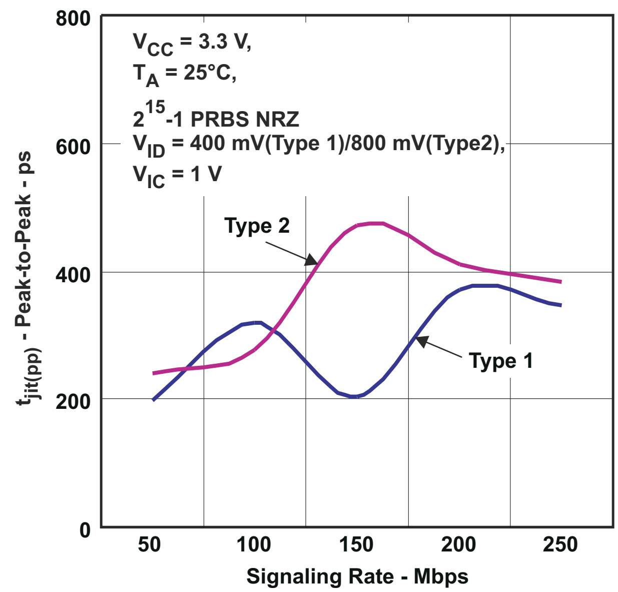


Figure 5-8. Added Receiver Peak-to-Peak Jitter vs Signaling Rate

5.9 Typical Characteristics (continued)

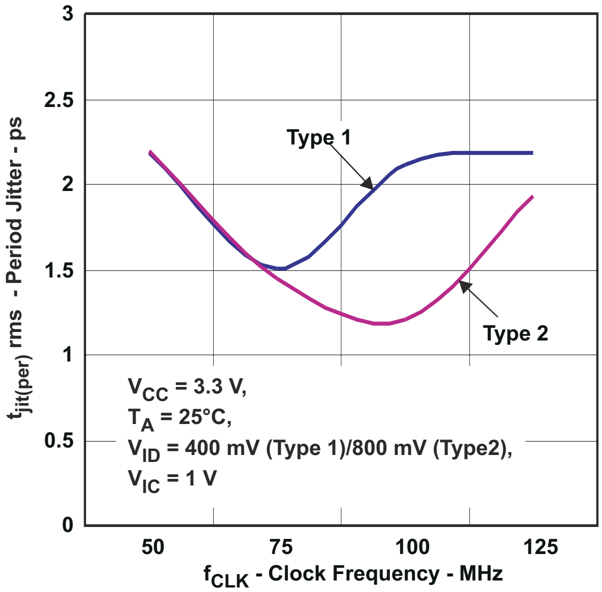


Figure 5-9. Added Receiver Period Jitter vs Clock Frequency

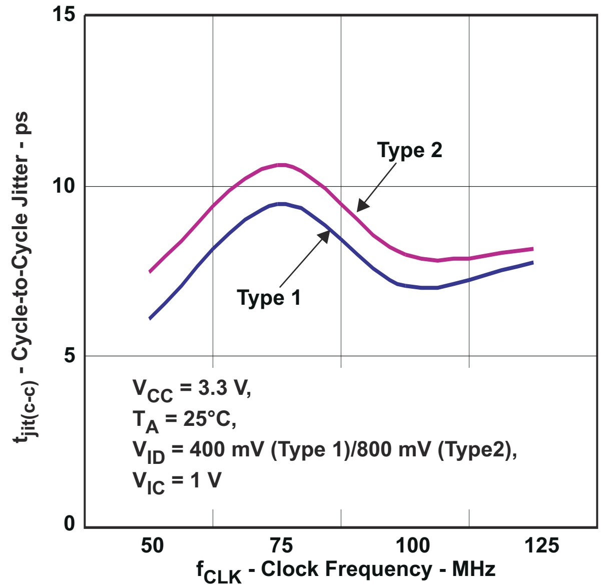


Figure 5-10. Added Receiver Cycle-to-Cycle Jitter vs Clock Frequency

5.9.1 Eye Patterns

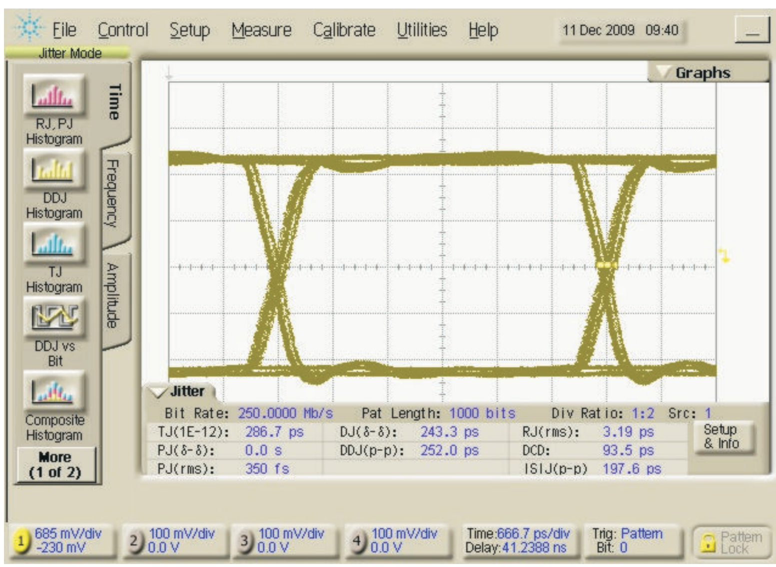


Figure 5-11. Output (V_{CC} = 3.3V, V_{ID} = 400mV) 250Mbps 2^{15}–1PRBS, Receiver Type 1

5.9.1 Eye Patterns (continued)

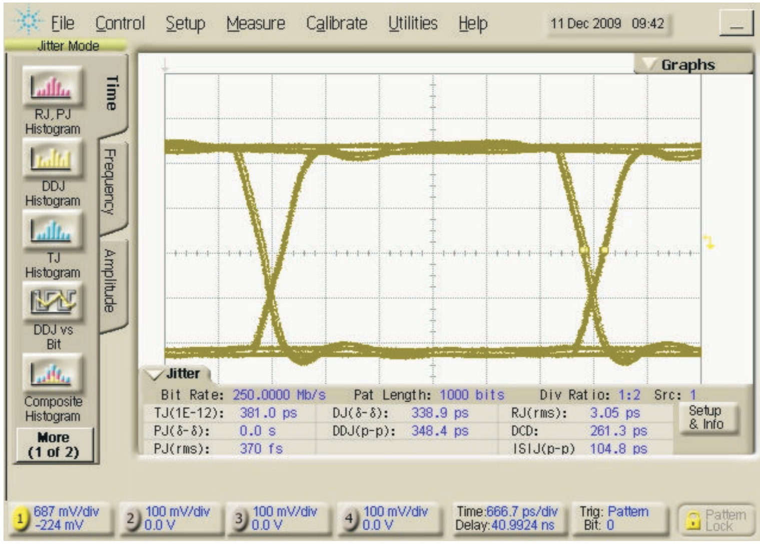


Figure 5-12. Output (V_{CC} = 3.3V, V_{ID} = 800mV) 250Mbps 2^{15}–1PRBS, Receiver Type 2

6 Parameter Measurement Information

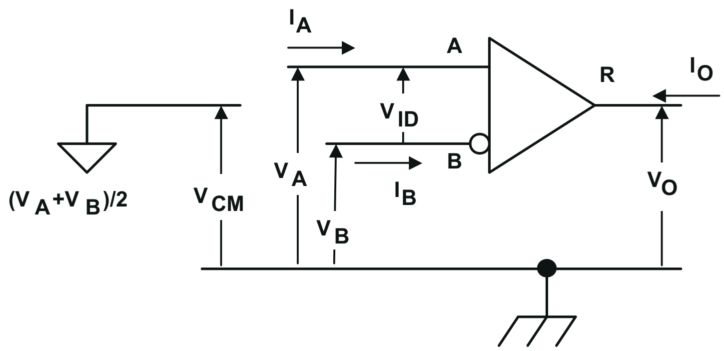


Figure 6-1. Receiver Voltage and Current Definitions

Table 6-1. Type-1 Receiver Input Threshold Test Voltages

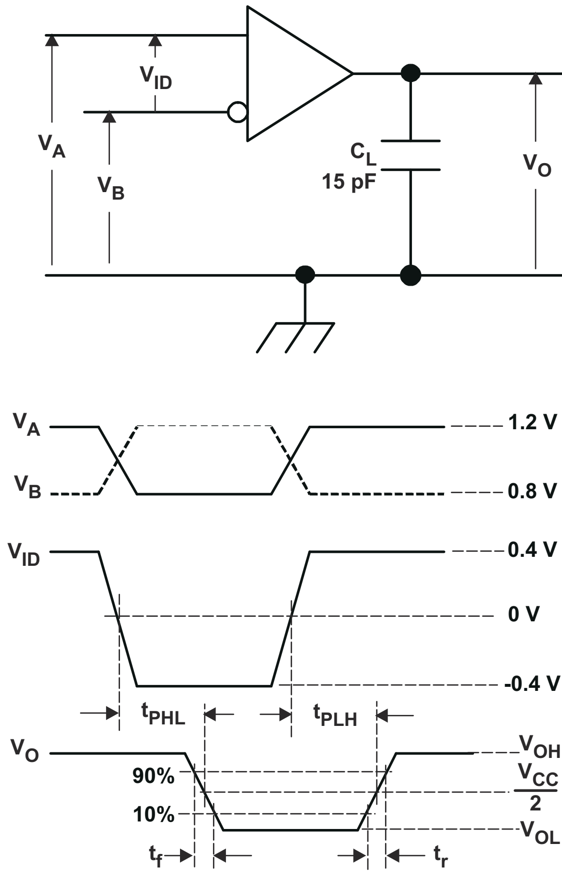
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.365	0.035	3.3825	H
3.365	3.400	–0.035	3.3825	L
–0.965	–1	0.035	–0.9825	H
–1	–0.965	–0.035	–0.9825	L

(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)

Table 6-2. Type-2 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT(1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	–2.400	1.200	L
3.400	3.265	0.135	3.3325	H
3.4000	3.335	0.05065	3.3675	L
–0.865	–1	0.135	–0.9325	H
-0.935	–1	0.065	–0.9675	L

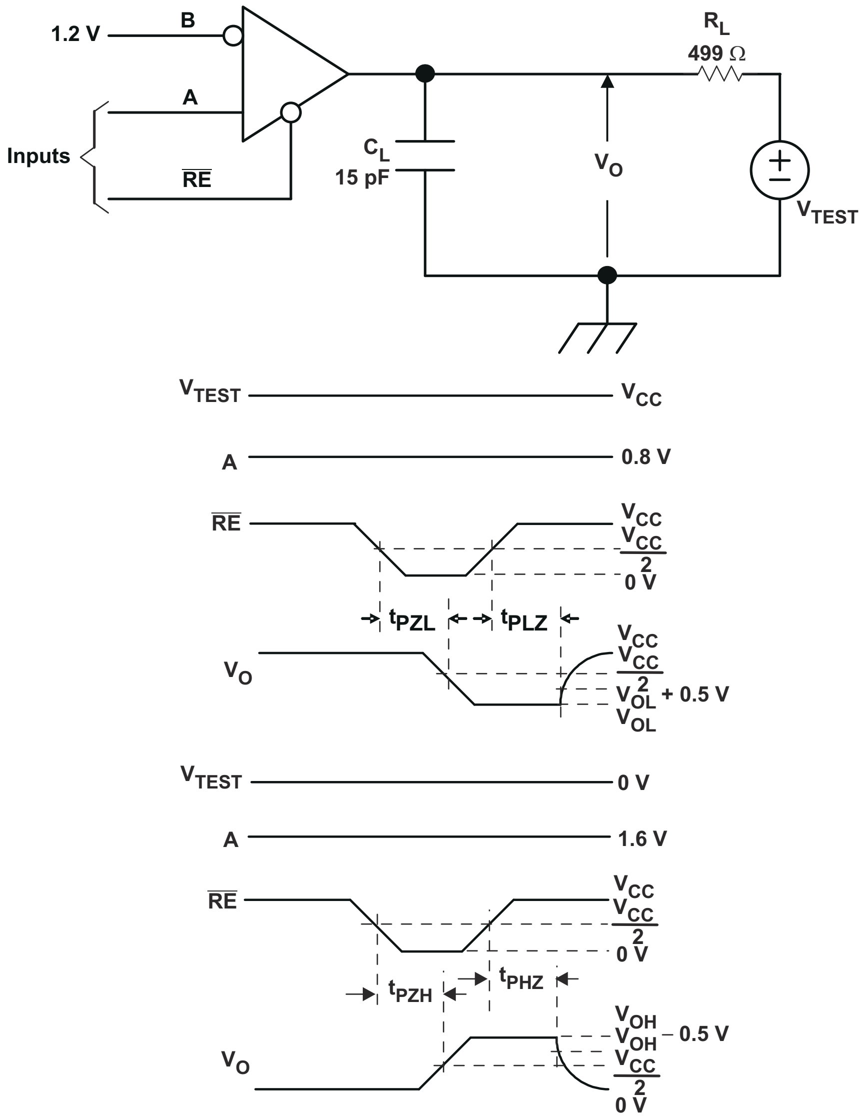
(1) H= high level, L = low level, output state assumes receiver is enabled ($\overline{RE}$ = L)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, Frequency = 1MHz, duty cycle = 50 ± 5%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

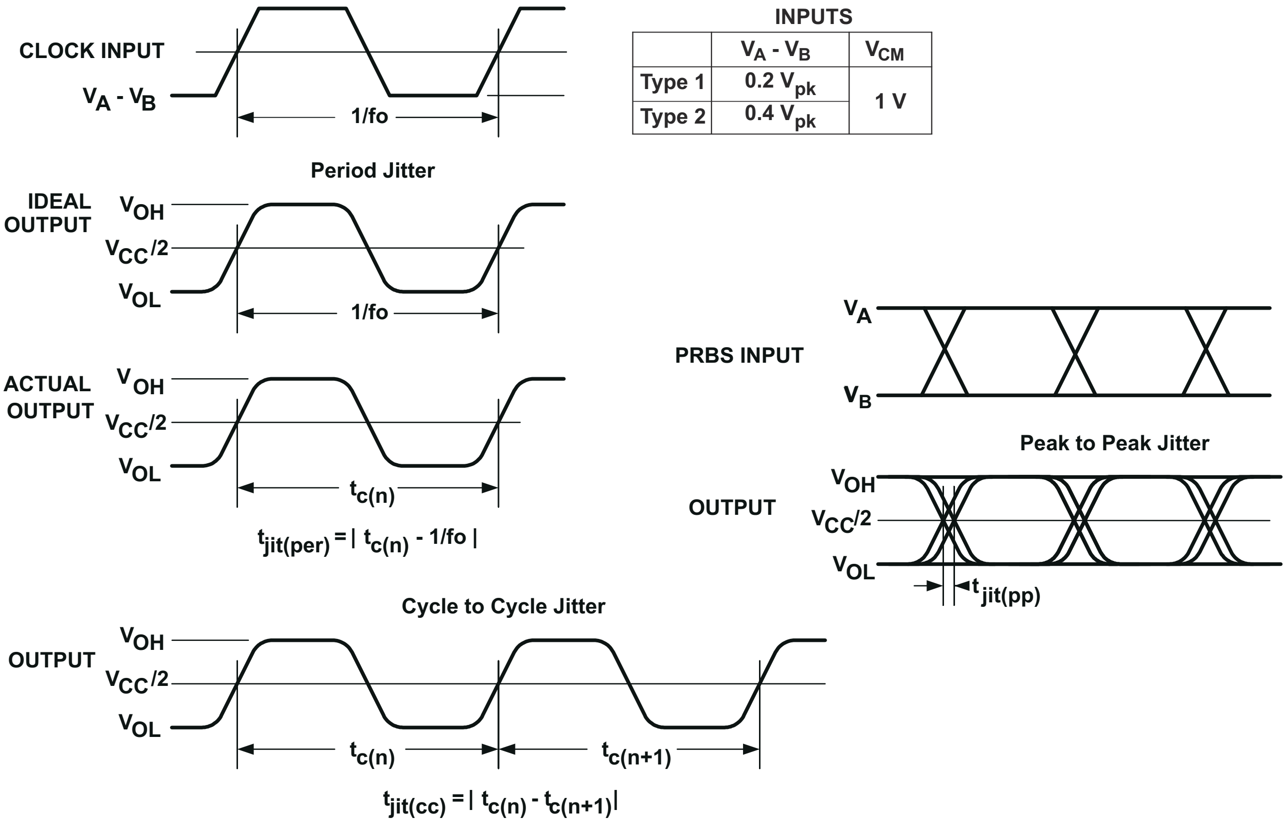
B. The measurement is made on test equipment with a –3dB bandwidth of at least 1GHz.

Figure 6-2. Receiver Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, frequency = 1MHz, duty cycle = 50 ± 5%.
B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T
C. C_L is the instrumentation and fixture capacitance within 2 cm of the D.U.T. and ±20%. The measurement is made on test equipment with a –3dB bandwidth of at least 1GHz.

Figure 6-3. Receiver Enable/Disable Time Test Circuit and Waveforms



INPUTS

	V_A - V_B	V_{CM}
Type 1	0.2 V_{pk}	1 V
Type 2	0.4 V_{pk}	

A. All input pulses are supplied by the Agilent 81250 Parallel BERT Stimulus System with plug-in E4832A.
B. The cycle-to-cycle jitter measurement is made on a TEK TDS6604 running TDSJIT3 application software.
C. All other jitter measurements are made with an Agilent Infiniium DCA-J 86100C Digital Communications Analyzer.
D. Period jitter and cycle-to-cycle jitter are measured using a 125MHz 50 ± 1% duty cycle clock input. Measured over 75K samples.
E. Deterministic jitter and random jitter are measured using a 250Mbps 2^{15} $^{-1}$ PRBS input. Measured over BER = 10^{-12}

Figure 6-4. Receiver Jitter Measurement Waveforms

7 Device Functional Modes

Table 7-1. Device Function Table

INPUTS[(1)]				RECEIVER TYPE	OUTPUT[(1)]
$V_{ID} = V_A - V_B$	PDN	FSEN	$\overline{RE}$		R
V_{ID} > 35mV	H	L	L	Type 1	H
–35mV ≤ V_{ID} ≤ 35mV	H	L	L	Type 1	?
V_{ID} < – 35mV	H	L	L	Type 1	L
V_{ID} > 135mV	H	H	L	Type 2	H
65mV ≤ V_{ID} ≤ 135mV	H	H	L	Type 2	?
V_{ID} < 65mV	H	H	L	Type 2	L
Open Circuit	H	L	L	Type 1	?
Open Circuit	H	H	L	Type 2	L
X	H	X	H	X	Z
X	H	X	OPEN	X	Z
X	L	X	X	X	Z

(1) H=high level, L=low level, Z=high impedance, X=Don't care, ?=indeterminate

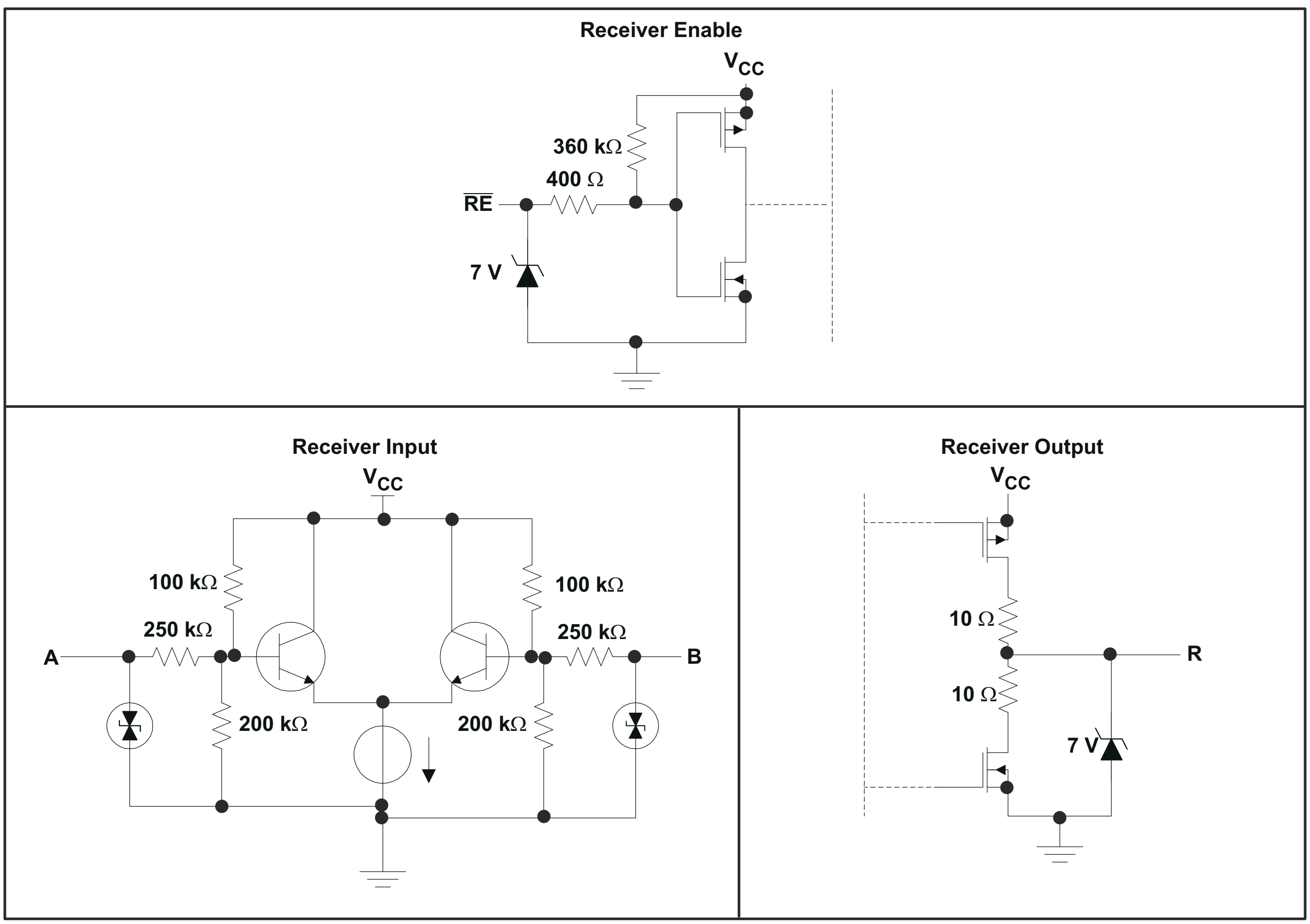


Figure 7-1. Equivalent Input and Output Schematic Diagrams

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2009) to Revision A (March 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document................	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD048RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	MLVD048	Samples
SN65MLVD048RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	MLVD048	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

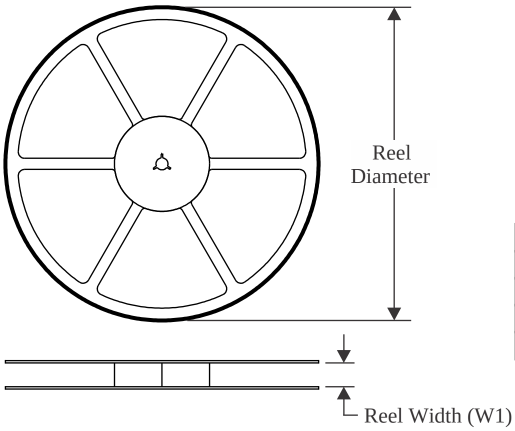
[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

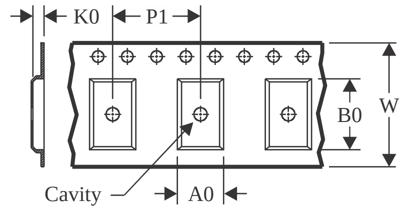
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

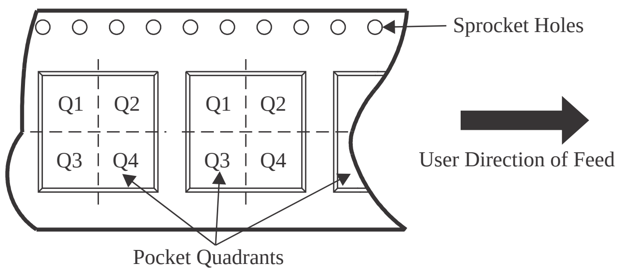


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

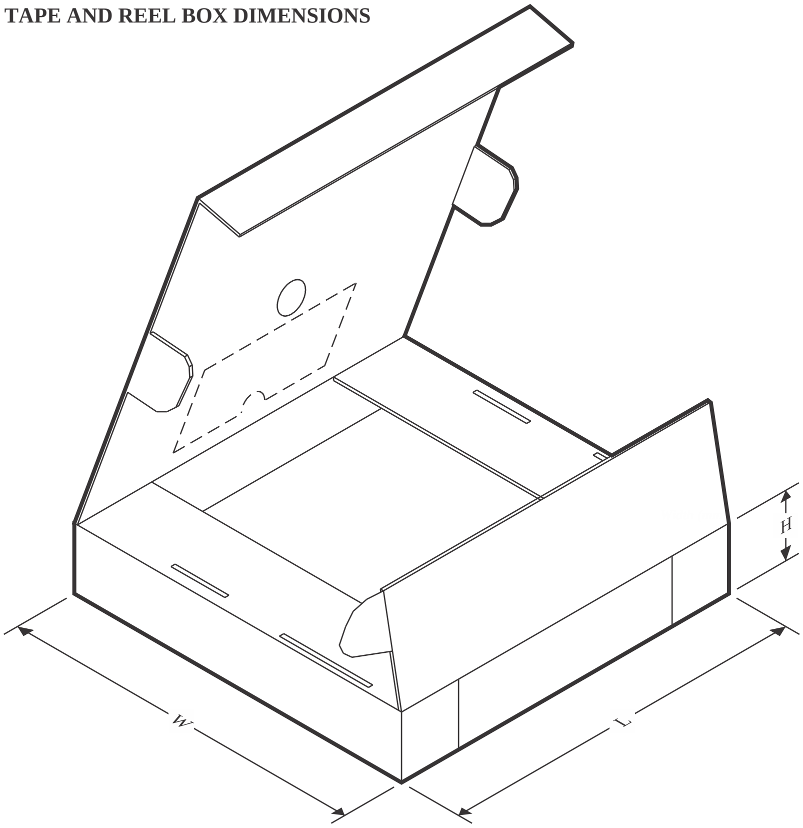
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD048RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN65MLVD048RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD048RGZR	VQFN	RGZ	48	2500	356.0	356.0	35.0
SN65MLVD048RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

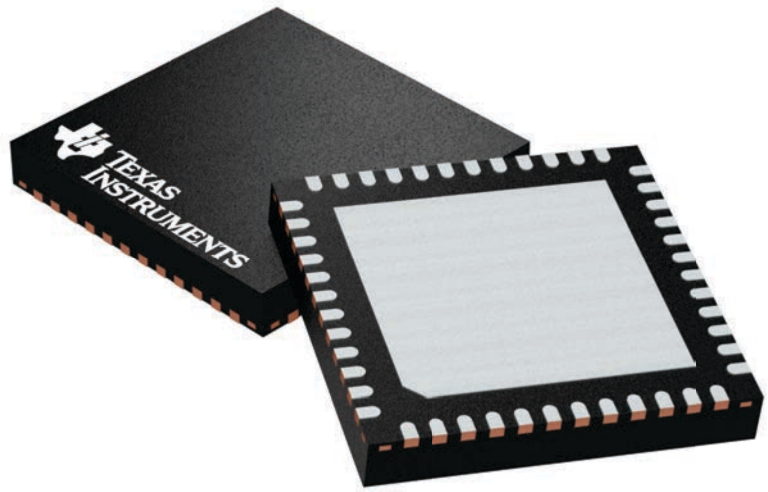
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

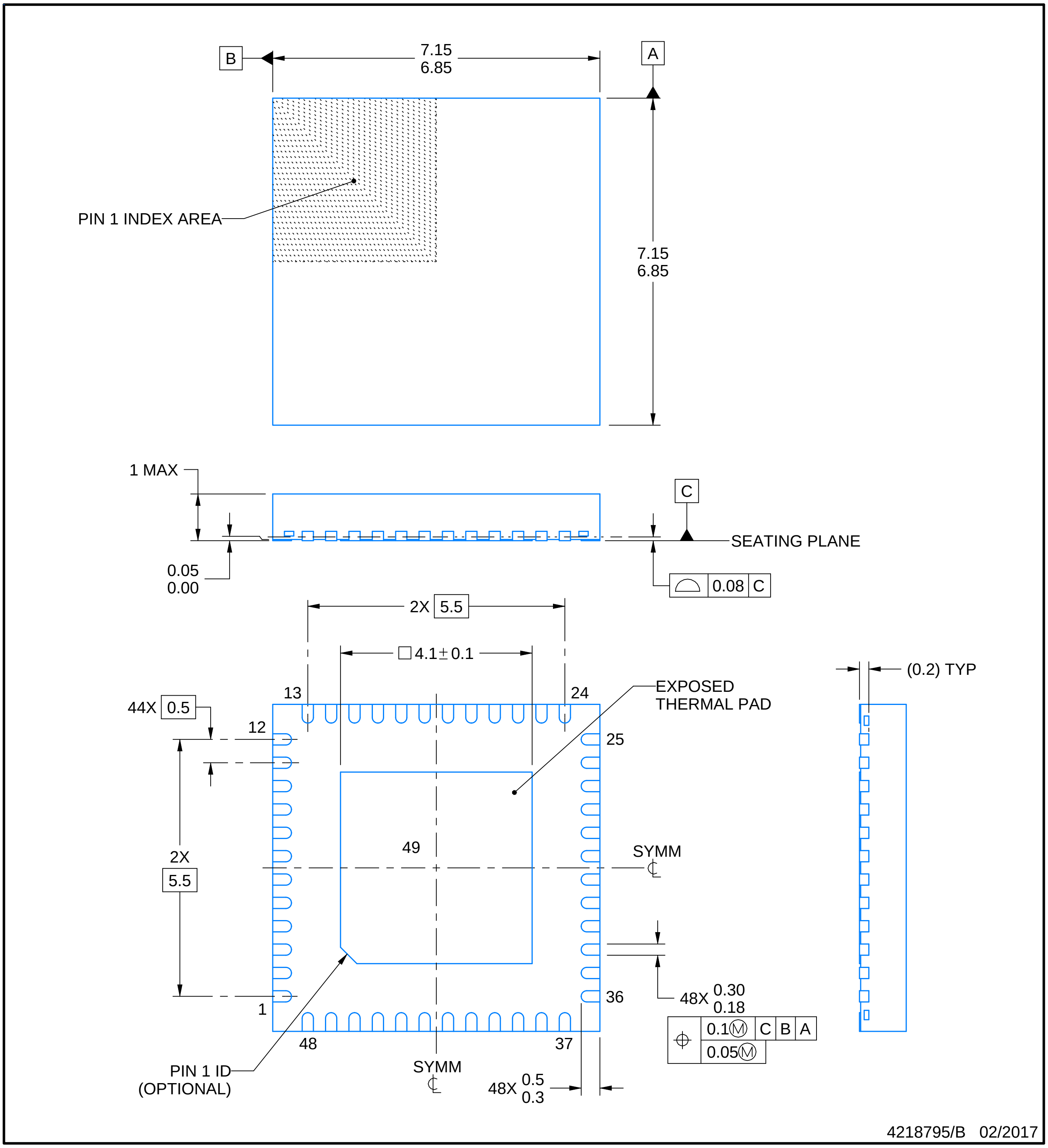
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



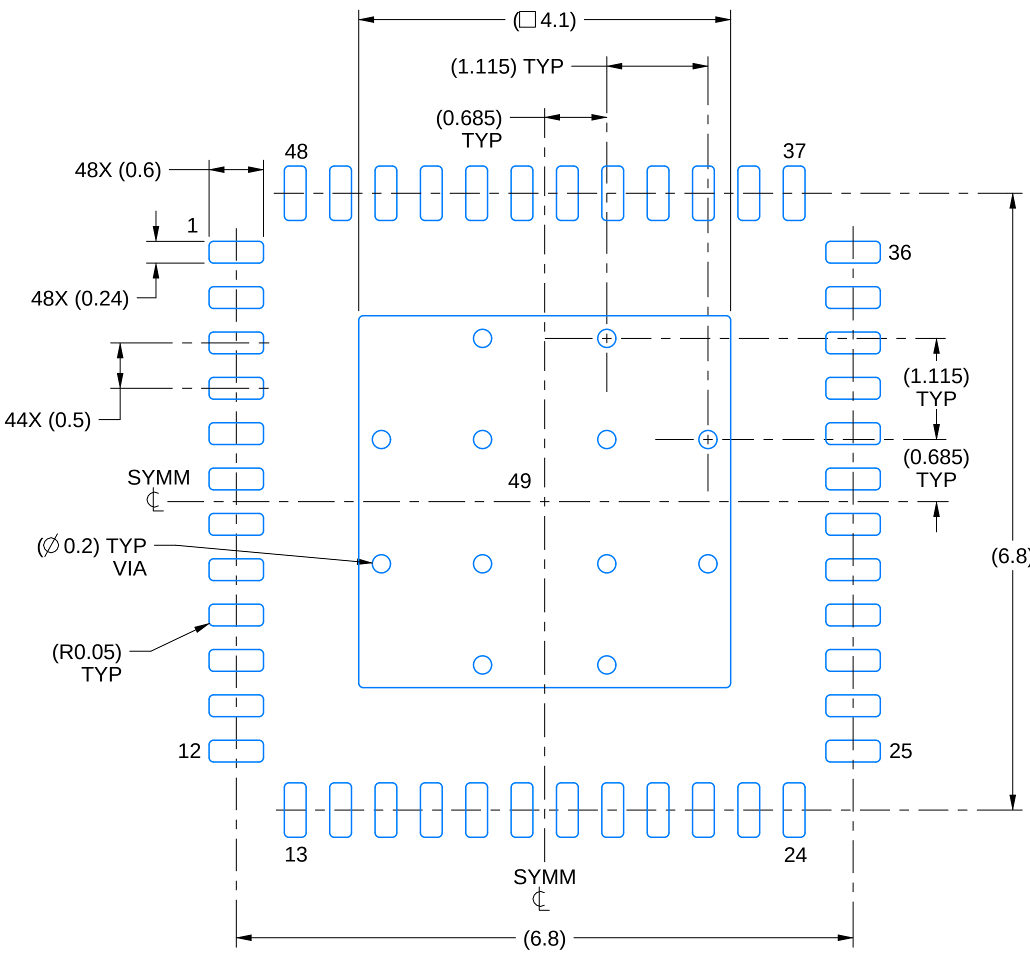
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

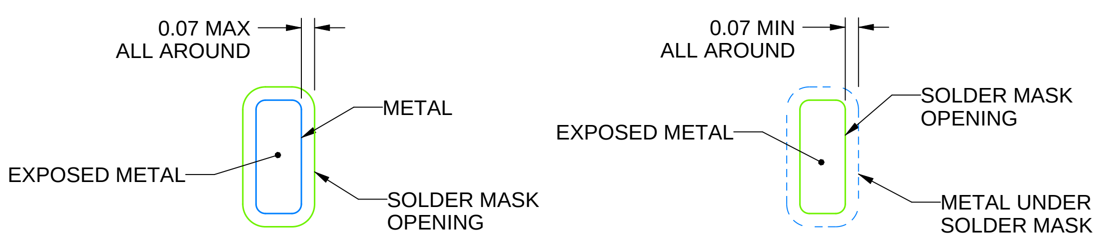


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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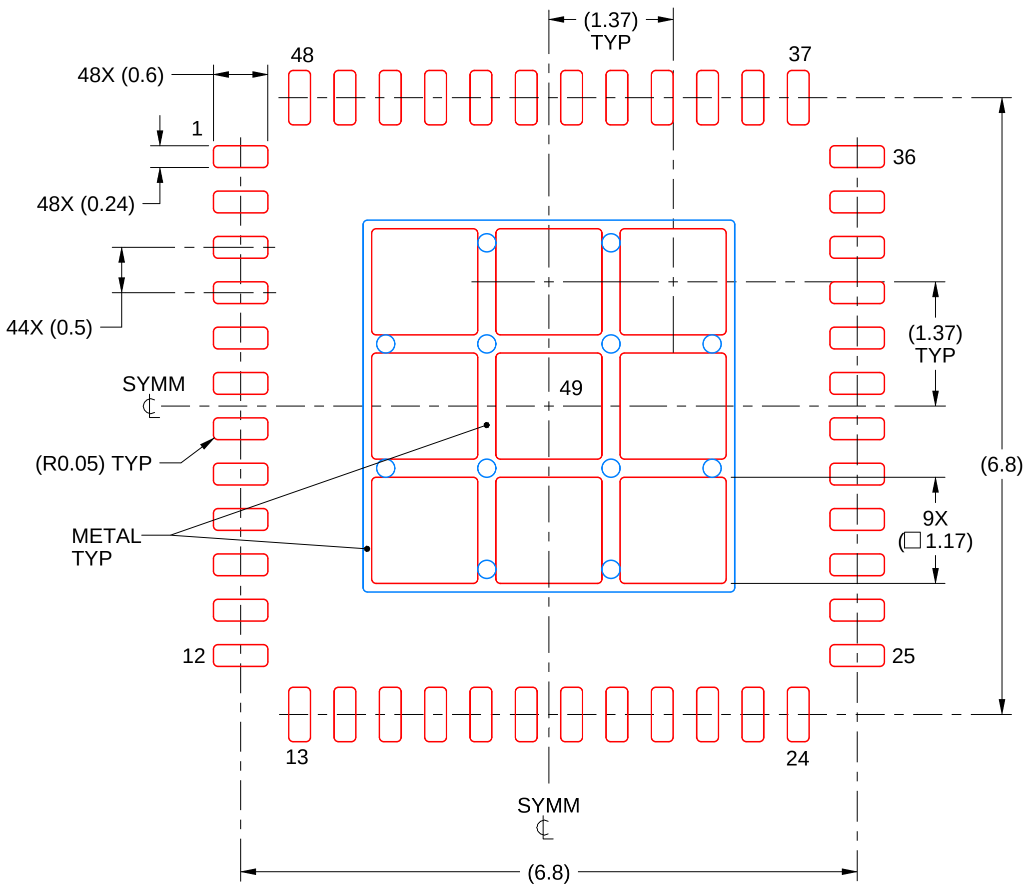
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.