

MC14528B

Dual Monostable Multivibrator

The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X .

Features

- Separate Reset Available
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- This part should only be used in new designs where the pulse width is $< 10 \mu s$
Note: For designs requiring a pulse width $> 10 \mu s$, please see MC14538, which is pin-for-pin compatible
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in}, V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I_{in}, I_{out}	± 10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C

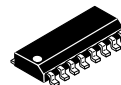
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



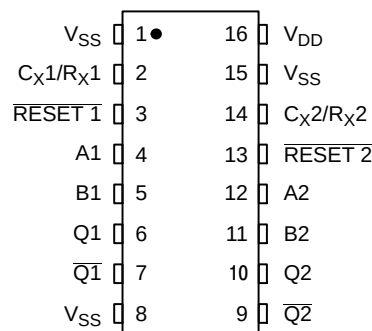
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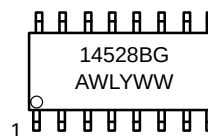


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SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



MARKING DIAGRAM



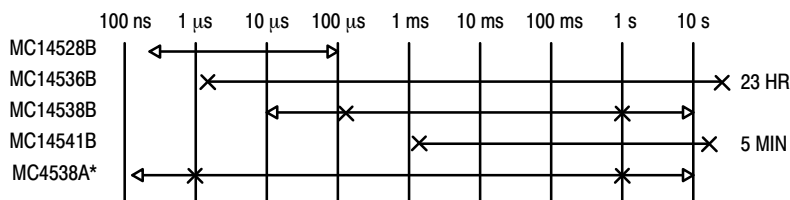
A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ONE-SHOT SELECTION GUIDE

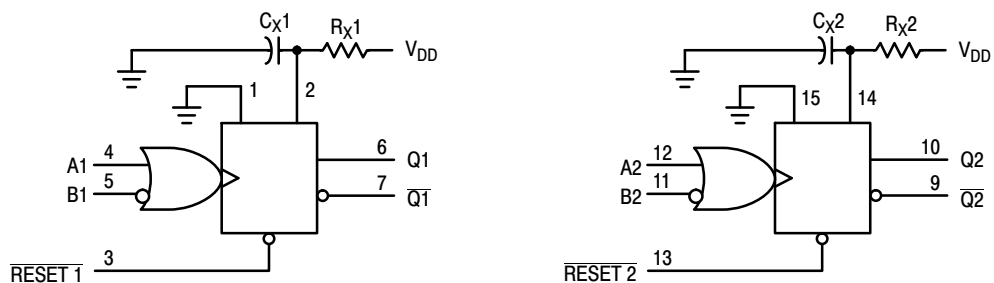


*LIMITED OPERATING VOLTAGE (2-6 V)

TOTAL OUTPUT PULSE WIDTH RANGE

RECOMMENDED PULSE WIDTH RANGE

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 1, PIN 8, PIN 15
R_X AND C_X ARE EXTERNAL COMPONENTS

FUNCTION TABLE

Inputs			Outputs	
Reset	A	B	Q	$\bar{Q}$
H H	 L	H 	 	 
H H	 L H	L 	Not Triggered Not Triggered	
H H	L, H,  L	H L, H, 	Not Triggered Not Triggered	
L 	X X	X X	L H Not Triggered	

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
“1” Level V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
“1” Level (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	I _{OH}	5.0	–1.2	–	–1.0	–1.7	–	–0.7	–	mAdc
		10	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current at an external load Capacitance (C _L) and at external timing capacitance (C _X), use the formula. (Note 3)	I _T	–	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2 \times 10^{-8} R_X C_X (V_{DD}^{-2})^2 f] \times 10^{-3}$ where: I _T in μA (per circuit), C _L and C _X in pF, R _X in megohms, V _{DD} in Vdc, f in kHz is input frequency.							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

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SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Note 4)

Characteristic	Symbol	C_X pF	R_X k Ω	V_{DD} Vdc	Min	Typ (Note 5)	Max	Unit
Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH} , t_{THL}	—	—	5.0 10 15	— — —	100 50 40	200 100 80	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\bar{Q}$ t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 240 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 87 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$	t_{PLH} , t_{PHL}	15	5.0	5.0 10 15	— — —	325 120 90	650 240 180	ns
Turn-Off, Turn-On Delay Time — A or B to Q or $\bar{Q}$ t_{PLH} , $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 620 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$ t_{PLH} , $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 185 \text{ ns}$	t_{PLH} , t_{PHL}	1000	10	5.0 10 15	— — —	705 290 210	— — —	ns
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0 10 15	150 75 55	70 30 30	— — —	ns
	t_{WL}	1000	10	5.0 10 15	— — —	70 30 30	— — —	ns
Output Pulse Width — Q or $\bar{Q}$ (For $C_X < 0.01 \mu\text{F}$ use graph for appropriate V_{DD} level.)	t_W	15	5.0	5.0 10 15	— — —	550 350 300	— — —	ns
Output Pulse Width — Q or $\bar{Q}$ (For $C_X > 0.01 \mu\text{F}$ use formula: $t_W = 0.2 R_X C_X \ln [V_{DD} - V_{SS}]$) (Note 6)	t_W	10,000	10	5.0 10 15	15 10 15	30 50 55	45 90 95	μs
Pulse Width Match between Circuits in the same package	$t_1 - t_2$	10,000	10	5.0 10 15	— — —	6.0 8.0 8.0	25 35 35	%
Reset Propagation Delay — $\overline{\text{Reset}}$ to Q or $\bar{Q}$	t_{PLH} , t_{PHL}	15	5.0	5.0 10 15	— — —	325 90 60	600 225 170	ns
		1000	10	5.0 10 15	— — —	1000 300 250	— — —	ns
Retrigger Time	t_{rr}	15	5.0	5.0 10 15	0 0 0	— — —	— — —	ns
		1000	10	5.0 10 15	0 0 0	— — —	— — —	ns
External Timing Resistance	R_X	—	—	—	5.0	—	1000	k Ω
External Timing Capacitance	C_X	—	—	—	No Limits (Note 7)			μF

4. The formulas given are for the typical characteristics only at 25°C .

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

6. If $C_X > 15 \mu\text{F}$, Use Discharge Protection Diode D_X , per Figure 9.

7. R_X is in Ω , C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

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ORDERING INFORMATION

Device	Package	Shipping [†]
MC14528BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14528BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
NLV14528BDR2G*	SOIC-16 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

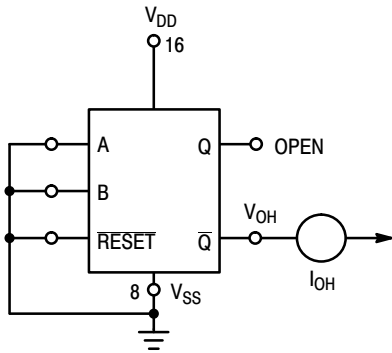


Figure 1. Output Source Current Test Circuit

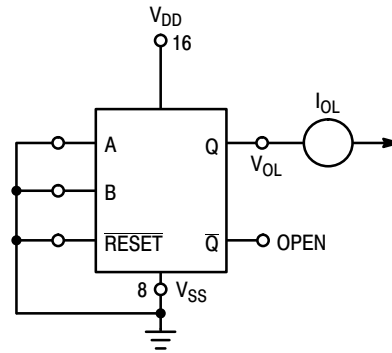


Figure 2. Output Sink Current Test Circuit

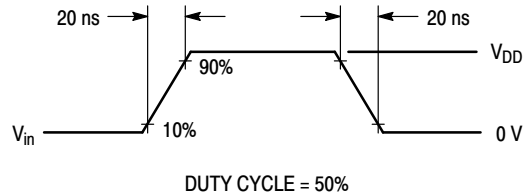
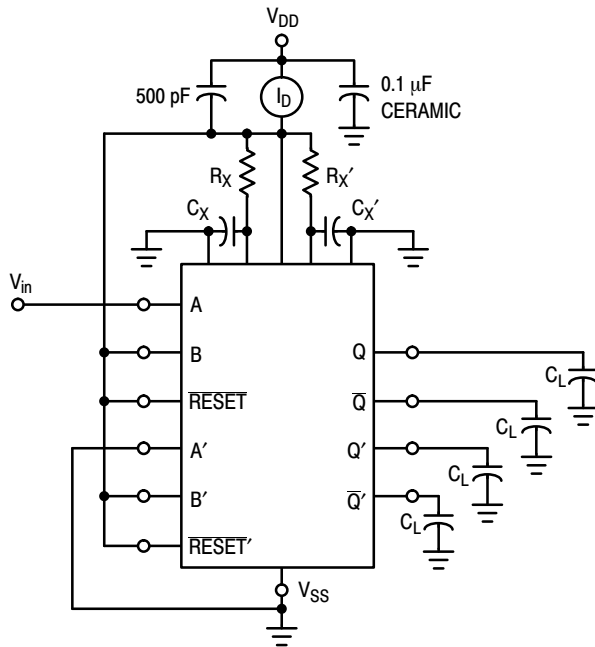
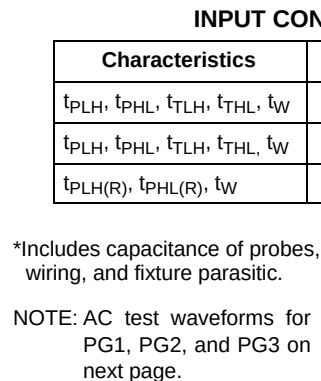


Figure 3. Power Dissipation Test Circuit and Waveforms

$$C_X = 15 \text{ pF}$$

$$C_L = 15 \text{ pF}$$

$$R_X = 5.0 \text{ k}\Omega$$


PG1 = 

PG2 = 

PG3 = 

[illegible]

This graph shows the relationship between pulse width (t_W) and external capacitance (C_X) for the 74VHC00. The y-axis represents pulse width in microseconds (μs) on a logarithmic scale from 0.1 to 1000. The x-axis represents external capacitance in picofarads (pF) on a logarithmic scale from 10 to 100,000. Three sets of curves are plotted for different load resistances: $R_X = 100\text{ k}\Omega$, $R_X = 10\text{ k}\Omega$, and $R_X = 5.0\text{ k}\Omega$. Within each set, curves are shown for supply voltages $V_{DD} = 5.0\text{ V}$, 10 V , and 15 V . The graph indicates that pulse width increases with both external capacitance and load resistance, and decreases with higher supply voltage.

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TYPICAL APPLICATIONS

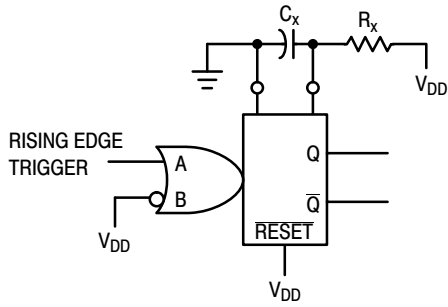


Figure 7. Retriggerable Monostables Circuitry

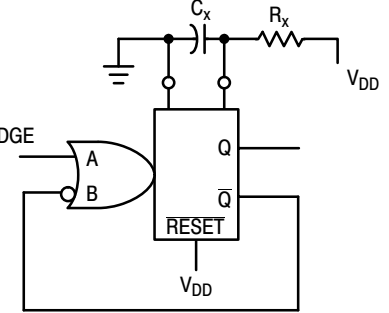
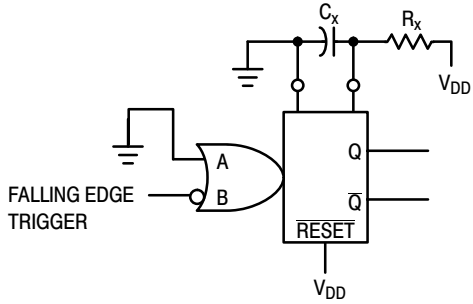


Figure 8. Non-Retriggerable Monostables Circuitry

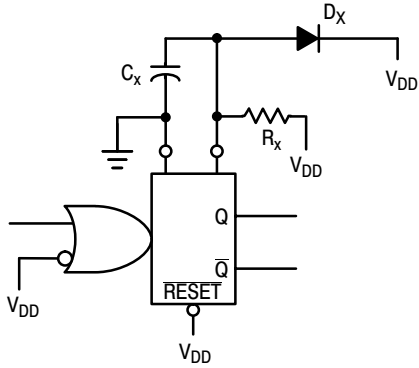


Figure 9. Use of a Diode to Limit Power Down Current Surge

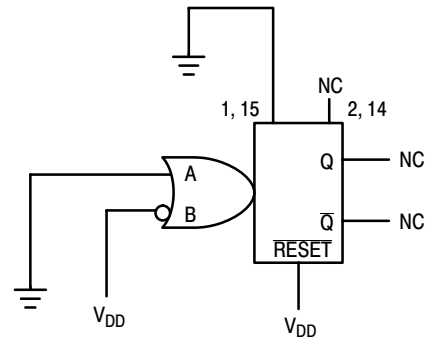
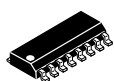


Figure 10. Connection of Unused Sections

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



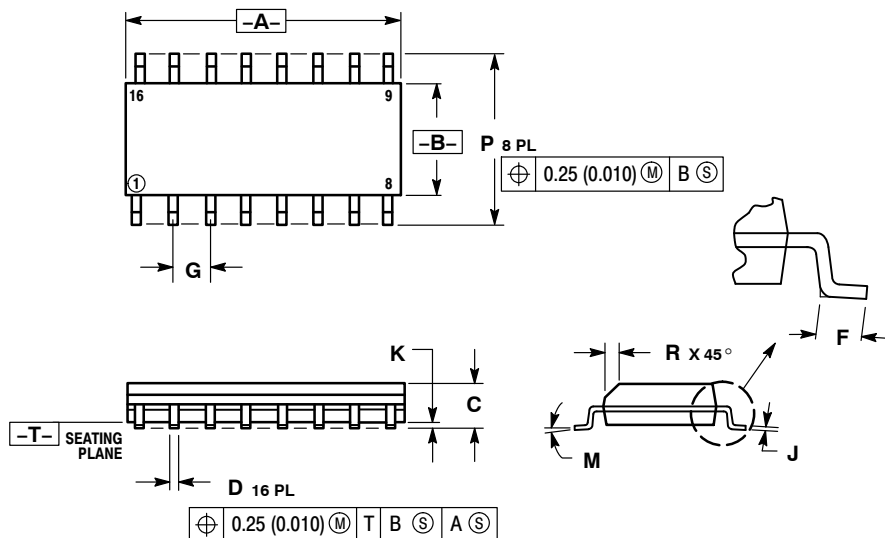
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CASE 751B-05

ISSUE K

DATE 29 DEC 2006



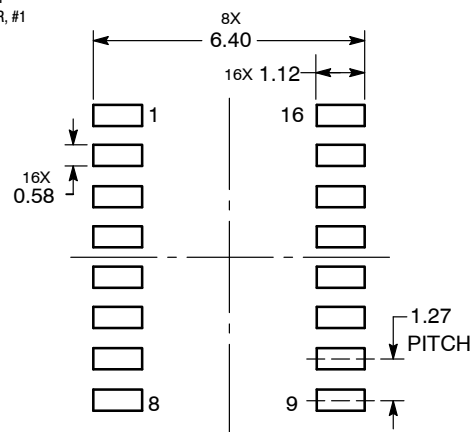
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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