

NUP4302MR6

Schottky Diode Array for Four Data Line ESD Protection

The NUP4302MR6 is designed to protect high speed data line interface from ESD, EFT and lightning.

Features

- Very Low Forward Voltage Drop
- Fast Switching
- PN Junction Guard Ring for Transient and ESD Protection
- ESD Rating of Class 3B (Exceeding 16 kV) per Human Body Model and Class C (Exceeding 400 V) per Machine Model
- IEC 61000-4-2 Level 4 ESD Protection
- Flammability Rating: UL 94 V-0
- Pb-Free Package is Available

Applications

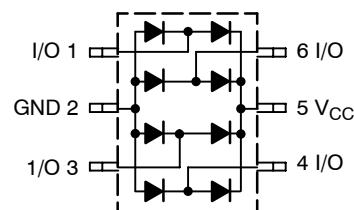
- Ultra High-Speed Switching
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI)
- Monitors and Flat Panel Displays



ON Semiconductor®

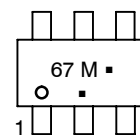
<http://onsemi.com>

PIN CONFIGURATION AND SCHEMATIC



**TSOP-6
CASE 318G
STYLE 12**

MARKING DIAGRAM



67 = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NUP4302MR6T1	TSOP-6	3000/Tape & Reel
NUP4302MR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NUP4302MR6

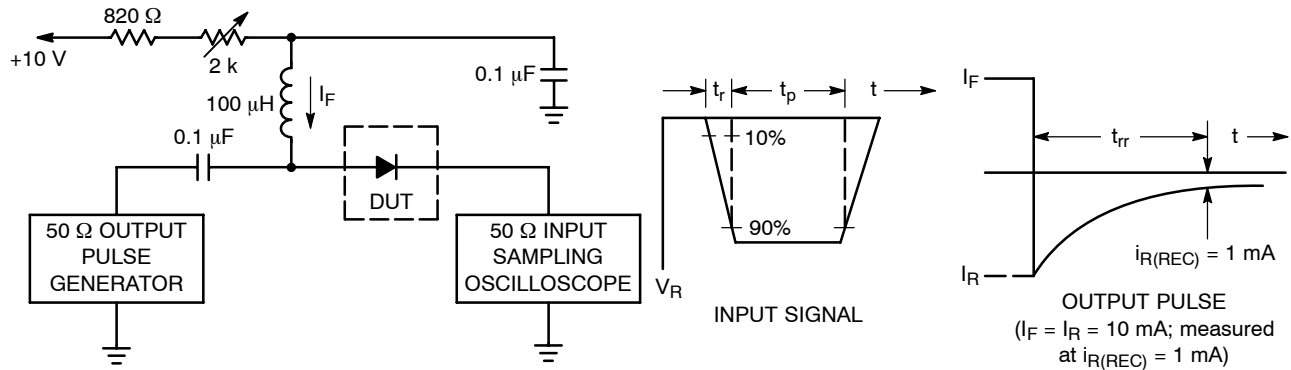
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Reverse Breakdown Voltage	V _{BR}	30	V
Forward Power Dissipation (T _A = 25°C)	P _F	225	mW
Forward Continuous Current	I _F	200	mA
Junction Operating Temperature	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Breakdown Voltage	V _{BR}	I _R = 100 μA	30			V
Reverse Leakage	I _R	V _R = 25 V			30	μA
Forward Voltage	V _F	I _F = 0.1 mAdc			0.28	V
Forward Voltage	V _F	I _F = 1.0 mAdc			0.35	V
Forward Voltage	V _F	I _F = 10 mAdc			0.45	V
Forward Voltage	V _F	I _F = 100 mAdc			1.00	V
Total Capacitance	C _T	V _R = 0 V, f = 1.0 MHz, I/O to Ground V _R = 0 V, f = 1.0 MHz, I/O to I/O			28 18	pF
Reverse Recovery Time	t _{rr}	I _F = I _R = 10 mA, I _{R(REC)} = 1.0 mA (Figure 1)			5.0	ns



- Notes: 1. A 2.0 kΩ variable resistor adjusted for a Forward Current (I_F) of 10 mA.
 2. Input pulse is adjusted so I_{R(peak)} is equal to 10 mA.
 3. t_p » t_{rr}

Figure 1. Recovery Time Equivalent Test Circuit

NUP4302MR6

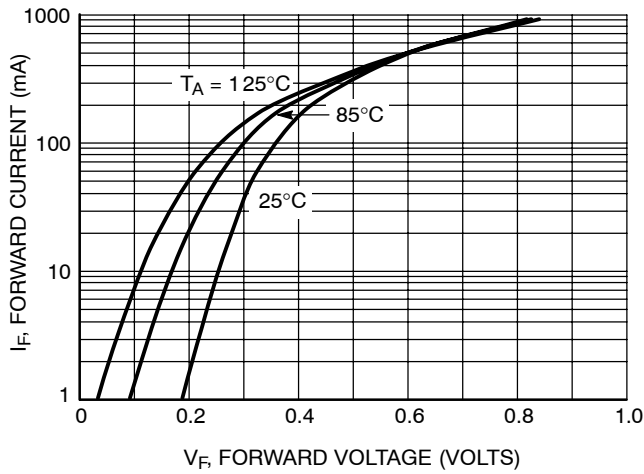


Figure 2. Forward Current as a Function of Forward Voltage; Typical Values

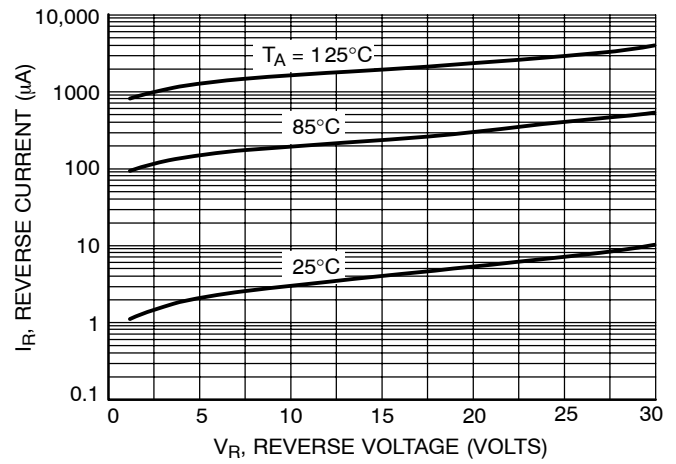


Figure 3. Reverse Current as a Function of Reverse Voltage; Typical Values

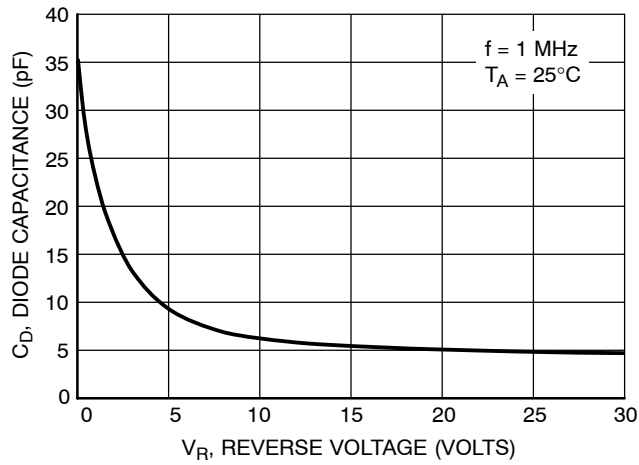
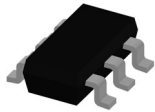


Figure 4. Diode Capacitance as a Function of Reverse Voltage; Typical Values

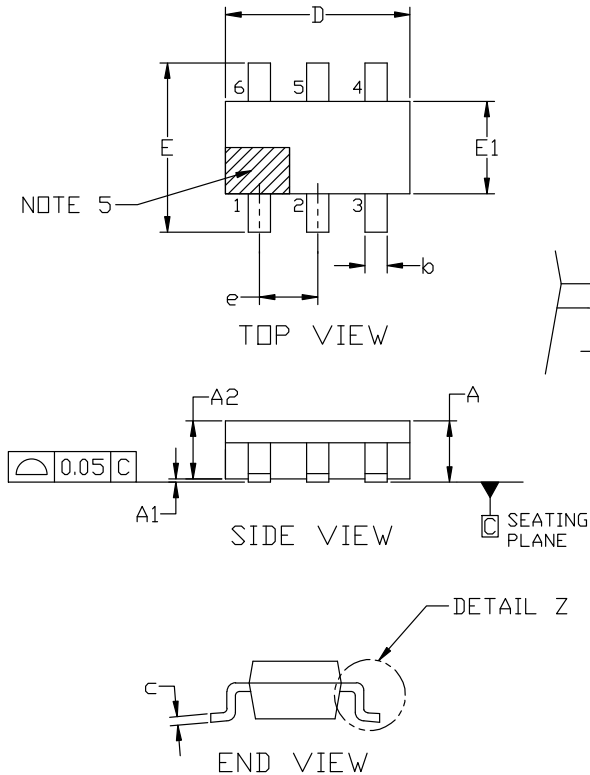


TSOP-6 3.00x1.50x0.90, 0.95P

CASE 318G

ISSUE W

DATE 26 FEB 2024

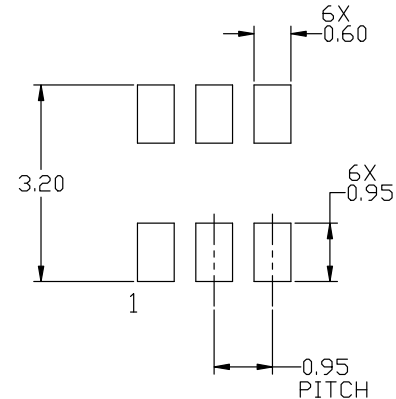


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS

DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



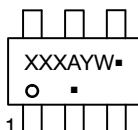
TSOP-6 3.00x1.50x0.90, 0.95P

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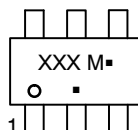
ISSUE W

DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

▪ = Pb-Free Package

XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:

PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:

PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:

PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:

PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:

PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:

PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:

PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:

PIN 1. D(OUT)+
2. GND
3. D(OUT)-
4. D(IN)-
5. VBUS
6. D(IN)+

STYLE 11:

PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:

PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:

PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:

PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:

PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:

PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:

PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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