NCP361, NCV361

USB Positive Overvoltage Protection Controller with Internal PMOS FET and Overcurrent Protection

The NCP361 disconnects systems at its output when wrong VBUS operating conditions are detected at its input. The system is positive over−voltage protected up to +20 V.

Thanks to an integrated PMOS FET, no external device is necessary, reducing the system cost and the PCB area of the application board.

The NCP361 is able to instantaneously disconnect the output from the input if the input voltage exceeds the overvoltage threshold (5.675 V). Thanks to an overcurrent protection, the integrated PMOS is turning off when the charge current exceeds current limit (see options in ordering information).

The NCP361 provides a negative going flag ($\overline{\text{FLAG}}$) output, which alerts the system that voltage, current or overtemperature faults have occurred.

In addition, the device has ESD−protected input (15 kV Air) when bypassed with a 1 μF or larger capacitor.

Features

- Overvoltage Protection up to 20 V
- On−chip PMOS Transistor
- Overvoltage Lockout (OVLO)
- Undervoltage Lockout (UVLO)
- Overcurrent Protection
- Alert $\overline{\text{FLAG}}$ Output
- $\overline{\text{EN}}$ Enable Pin
- Thermal Shutdown
- Compliance to IEC61000−4−2 (Level 4)
  8 kV (Contact)
  15 kV (Air)
- ESD Ratings: Machine Model = B
  Human Body Model = 2
- UDFN6 2x2 mm and TSOP−5 3x3 mm Packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This is a Pb−Free Device

Applications

- USB Devices
- Mobile Phones
- Peripheral
- Personal Digital Applications
- MP3 Players
- Set Top Boxes

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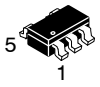
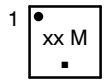
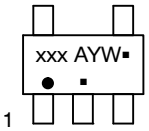
6 PIN UDFN
CASE 517AB



TSOP−5
CASE 483

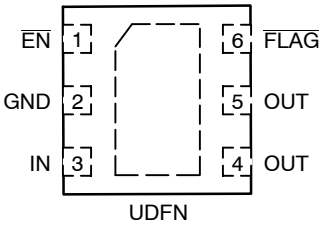
MARKING DIAGRAMS



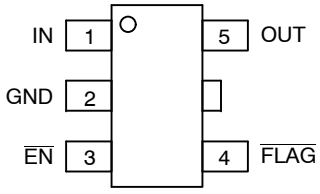


xxx = Specific Device Code
M = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



UDFN



TSOP−5

(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

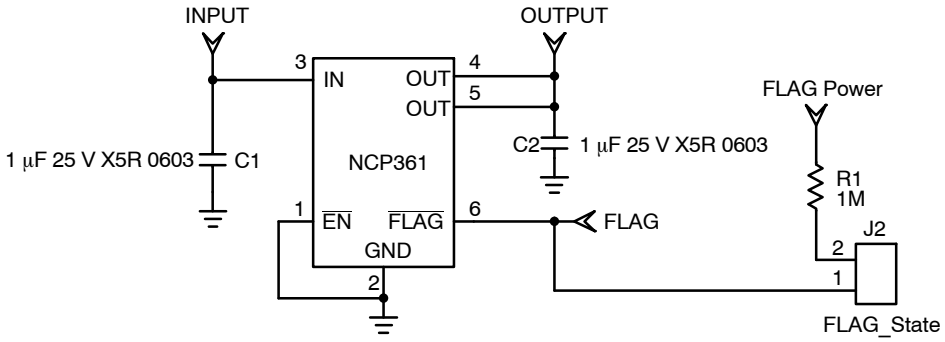


Figure 1. Typical Application Circuit (UDFN Pinout)

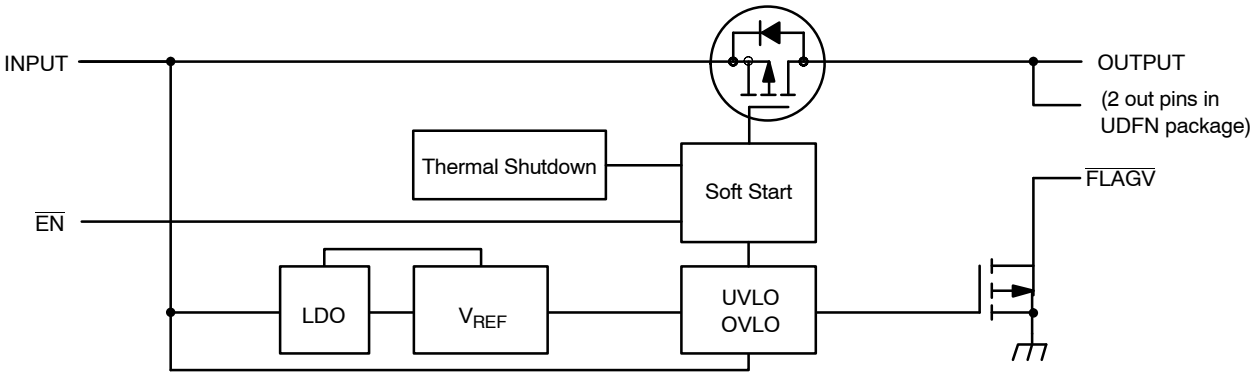


Figure 2. Functional Block Diagram

PIN FUNCTION DESCRIPTION (UDFN Package)

Pin No.	Name	Type	Description
1	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.
2	GND	POWER	Ground
3	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
4, 5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to these pins. The two OUT pins must be hardwired to common supply.
6	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.

PIN FUNCTION DESCRIPTION (TSOP−5 Package)

Pin No.	Name	Type	Description
1	IN	POWER	Input Voltage Pin. This pin is connected to the VBUS. A 1 μF low ESR ceramic capacitor, or larger, must be connected between this pin and GND.
2	GND	POWER	Ground
3	$\overline{EN}$	INPUT	Enable Pin. The device enters in shutdown mode when this pin is tied to a high level. In this case the output is disconnected from the input. To allow normal functionality, the $\overline{EN}$ pin shall be connected to GND or to a I/O pin. This pin does not have an impact on the fault detection.
4	$\overline{FLAG}$	OUTPUT	Fault Indication Pin. This pin allows an external system to detect a fault on VBUS pin. The $\overline{FLAG}$ pin goes low when input voltage exceeds OVLO threshold. Since the $\overline{FLAG}$ pin is open drain functionality, an external pull up resistor to V_{CC} must be added.
5	OUT	OUTPUT	Output Voltage Pin. The output is disconnected from the VBUS power supply when the input voltage is above OVLO threshold or below UVLO threshold. A 1 μF capacitor must be connected to this pin.

NOTE: Pin out provided for concept purpose only and might change in the final product

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Minimum Voltage (IN to GND)		$Vmin_{in}$	−0.3	V
Minimum Voltage (All others to GND)		Vmin	−0.3	V
Maximum Voltage (IN to GND)		$Vmax_{in}$	21	V
Maximum Voltage (All others to GND)		Vmax	7.0	V
Maximum DC Current from Vin to Vout (PMOS) (Note 1)		Imax	600	mA
Thermal Resistance, Junction−to−Air	TSOP−5 UDFN	$R_{\theta JA}$	305 240	°C/W
Operating Ambient Temperature Range		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Junction Operating Temperature		T_J	150	°C
ESD Withstand Voltage (IEC 61000−4−2) Human Body Model (HBM), Model = 2 (Note 2) Machine Model (MM) Model = B (Note 3)		Vesd	15 Air, 8.0 Contact 2000 200	kV V V
Moisture Sensitivity		MSL	Level 1	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. With minimum PCB area. By decreasing $R_{\theta JA}$, the current capability increases. See PCB recommendation page 9.
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114.
3. Machine Model, 200 pF discharged through all pins following specification JESD22/A115.

ELECTRICAL CHARACTERISTICS

(Min/Max limits values (−40°C < T_A < +85°C) and V_{in} = +5.0 V. Typical values are T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{in}		1.2		20	V
Undervoltage Lockout Threshold	UVLO	V_{in} falls down UVLO threshold	2.85	3.0	3.15	V
Uvervoltage Lockout Hysteresis	$UVLO_{hyst}$		50	70	90	mV
Overvoltage Lockout Threshold	OVLO	V_{in} rises up OVLO threshold	5.43	5.675	5.9	V
Overvoltage Lockout Hysteresis	$OVLO_{hyst}$		50	100	125	mV
V_{in} versus V_{out} Dopout	V_{drop}	V_{in} = 5 V, I charge = 500 mA		150	200	mV
Overcurrent Limit	I_{lim}	V_{in} = 5 V	550	750	950	mA
Supply Quiescent Current	Idd	No Load, V_{in} = 5.25 V		20	35	μA
Standby Current	I_{std}	V_{in} = 5 V, EN = 1.2 V		26	37	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.08		μA
FLAG Output Low Voltage	Vol_{flag}	V_{in} > OVLO Sink 1 mA on FLAG pin			400	mV
FLAG Leakage Current	$FLAG_{leak}$	FLAG level = 5 V		5.0		nA
$\overline{EN}$ Voltage High	V_{ih}	V_{in} from 3.3 V to 5.5 V	1.2			V
$\overline{EN}$ Voltage Low	V_{il}	V_{in} from 3.3 V to 5.5 V			0.55	V
EN Leakage Current	EN_{leak}	EN = 5.5 V or GND		170		nA
TIMINGS						
Start Up Delay	t_{on}	From V_{in} > UVLO to V_{out} = 0.8xV_{in}, See Fig 3 & 9		4.0	15	ms
FLAG going up Delay	t_{start}	From V_{in} > UVLO to FLAG = 1.2 V, See Fig 3 & 10		3.0		μs
Output Turn Off Time	t_{off}	From V_{in} > OVLO to V_{out} ≤ 0.3 V, See Fig 4 & 11 V_{in} increasing from 5 V to 8 V at 3 V/μs. No output capacitor.		0.7	1.5	μs
Alert Delay	t_{stop}	From V_{in} > OVLO to FLAG ≤ 0.4 V, See Fig 4 & 12 V_{in} increasing from 5 V to 8 V at 3 V/μs		1.0		μs
Disable Time	t_{dis}	From $\overline{EN}$ 0.4 to 1.2V to V_{out} ≤ 0.3 V, See Fig 5 & 13 V_{in} = 4.75 V. No output capacitor.		3.0		μs
Thermal Shutdown Temperature	T_{sd}			150		°C
Thermal Shutdown Hysteresis	T_{sdhyst}			30		°C

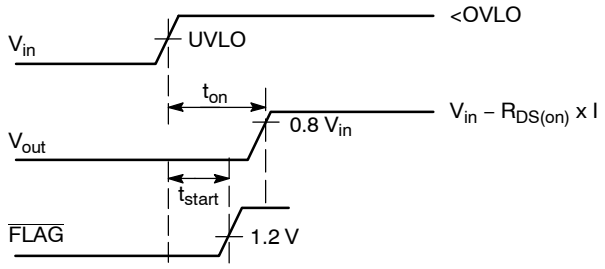


Figure 3. Start Up Sequence

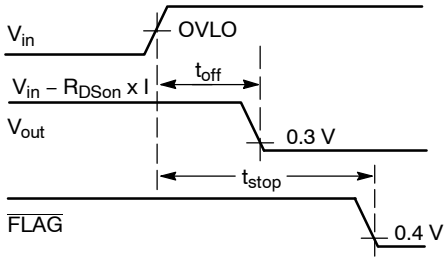


Figure 4. Shutdown on Over Voltage Detection

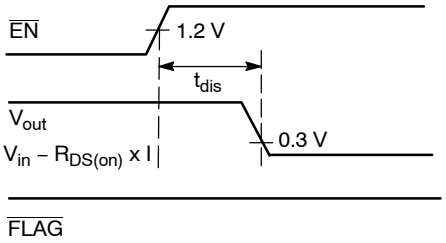


Figure 5. Disable on $\overline{EN}$ = 1

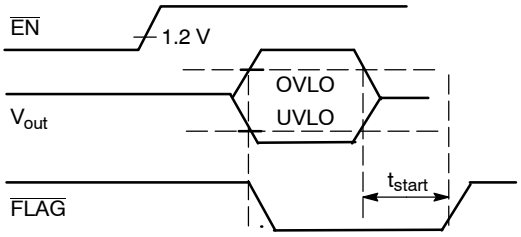


Figure 6. $\overline{FLAG}$ Response with $\overline{EN}$ = 1

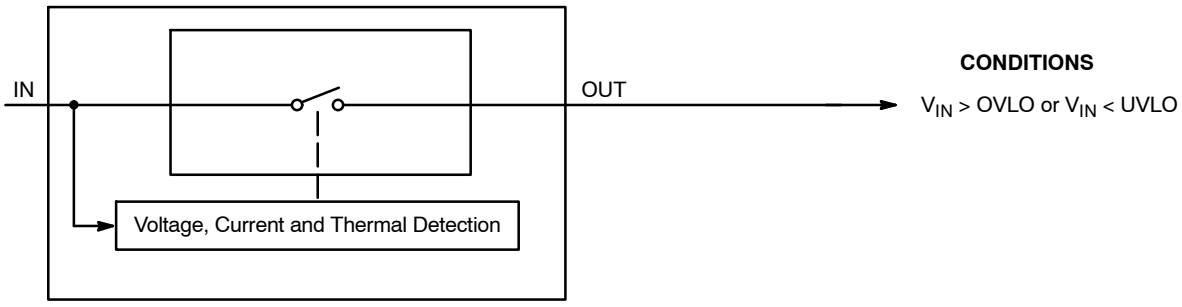


Figure 7.

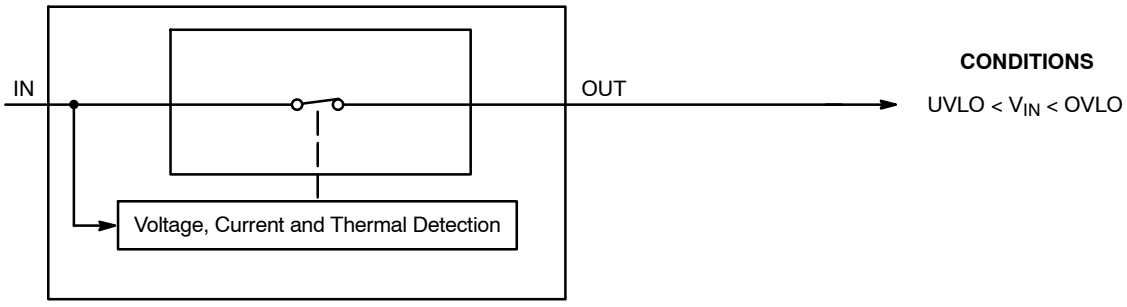


Figure 8.

TYPICAL OPERATING CHARACTERISTICS

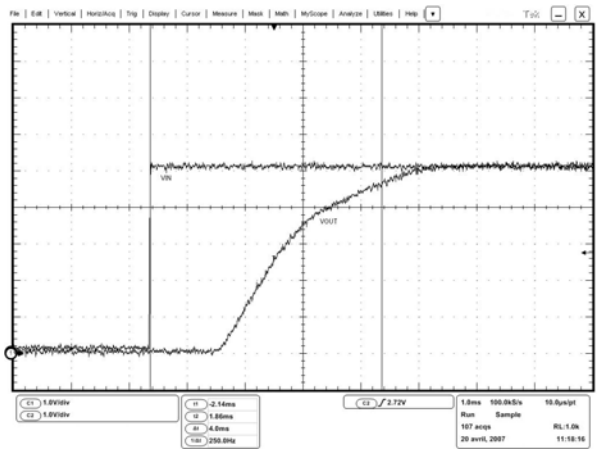


Figure 9. Start Up. Vin=Ch1, Vout=Ch2

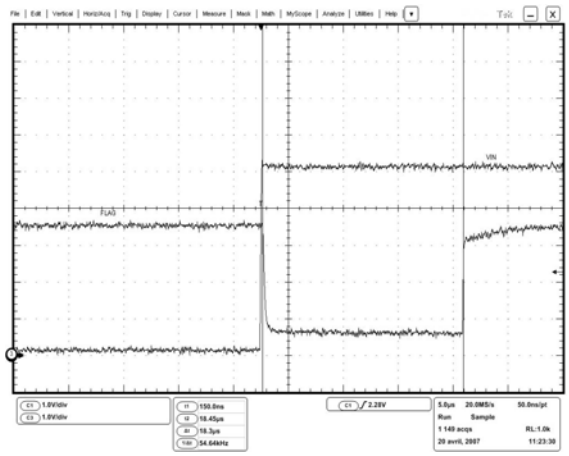


Figure 10. FLAG Going Up Delay. Vin=Ch1, FL:AG=Ch3

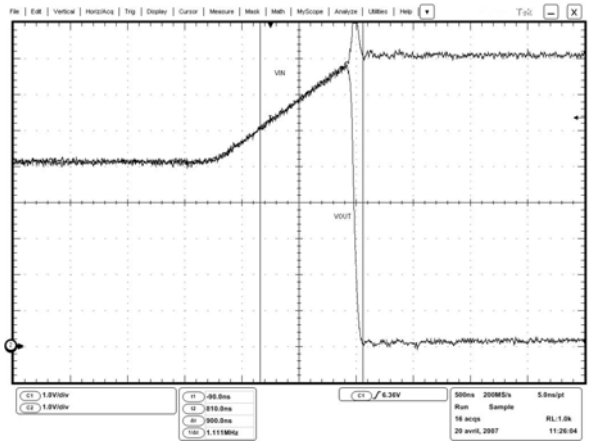


Figure 11. Output Turn Off time. Vin=Ch1, Vout=Ch2

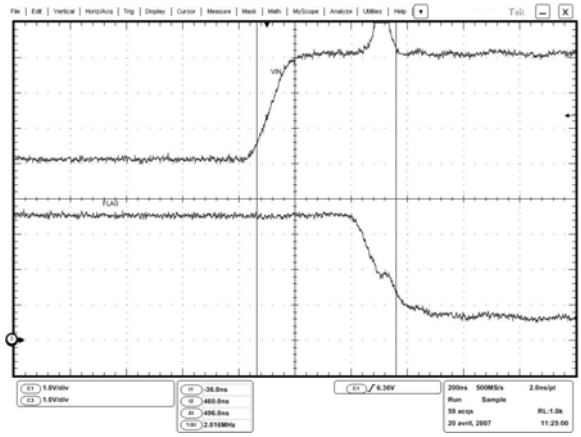


Figure 12. Alert Delay. Vout=Ch1, FLAG=Ch3

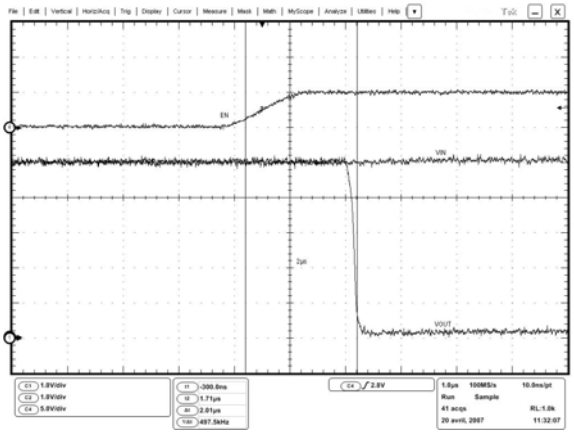


Figure 13. Disable Time. EN=Ch4, Vin=Ch1, Vout=Ch2

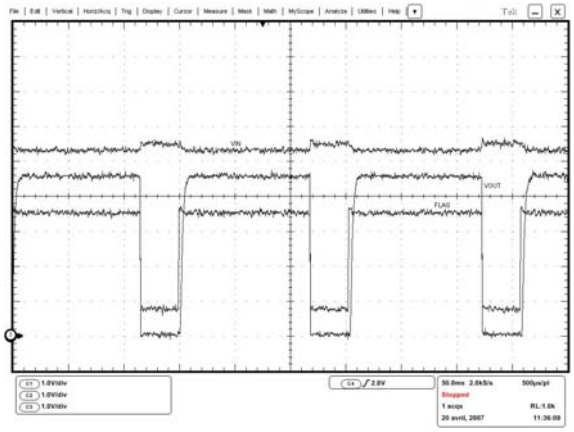


Figure 14. Thermal Shutdown. Vin=Ch1, Vout=Ch2, FLAG=Ch3

TYPICAL OPERATING CHARACTERISTICS

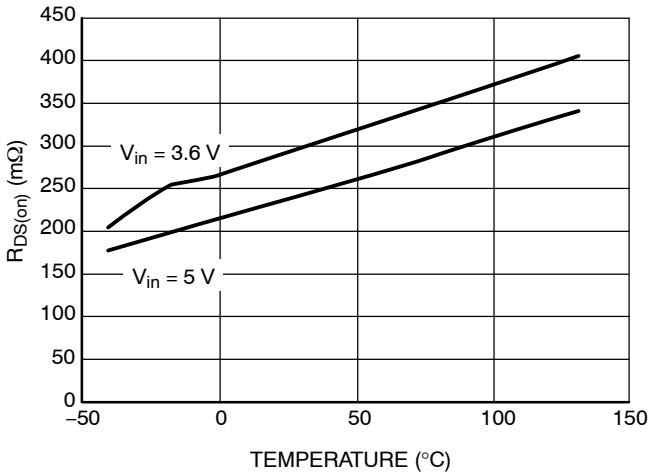


Figure 15. $R_{DS(on)}$ vs. Temperature (Load = 500 mA)

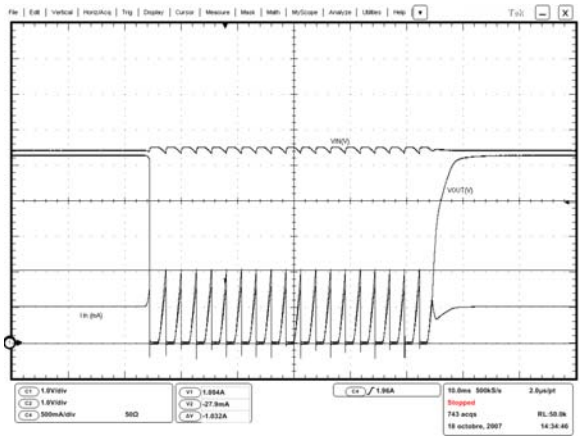


Figure 16. Output Short Circuit

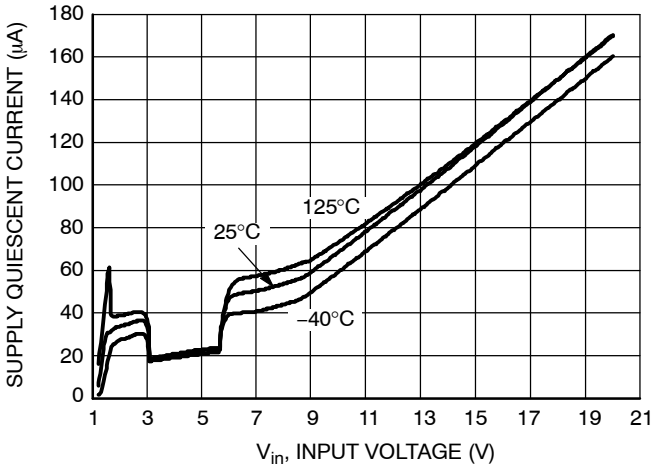


Figure 17. Quiescent Current vs. Input Voltage

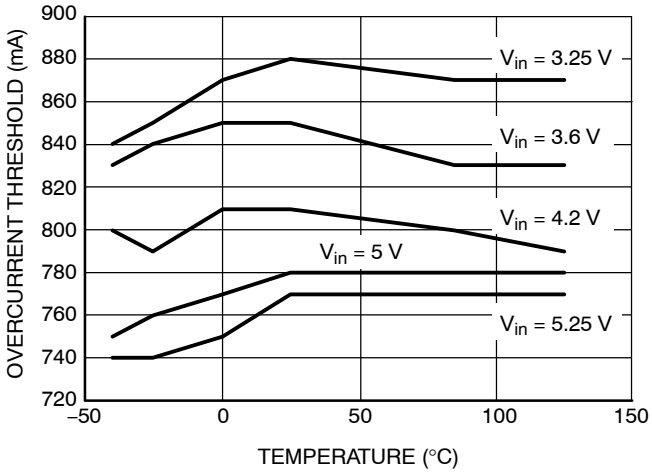


Figure 18. Overcurrent Protection Threshold vs. Temperature

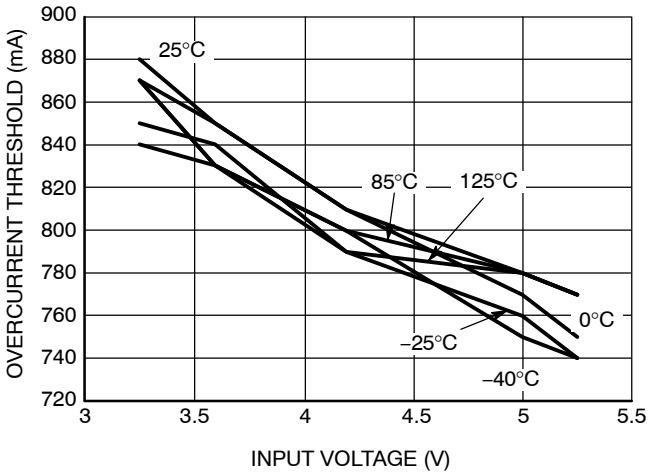


Figure 19. Overcurrent Protection Threshold vs. Input Voltage

Operation

NCP361 provides overvoltage protection for positive voltage, up to 20 V. A PMOS FET protects the systems (i.e.: VBUS) connected on the V_{out} pin, against positive overvoltage. The Output follows the VBUS level until OVLO threshold is overtaken.

Undervoltage Lockout (UVLO)

To ensure proper operation under any conditions, the device has a built−in undervoltage lock out (UVLO) circuit. During V_{in} positive going slope, the output remains disconnected from input until V_{in} voltage is above 3.0 V nominal. The $\overline{FLAGV}$ output is pulled to low as long as V_{in} does not reach UVLO threshold. This circuit has a 70 mV hysteresis to provide noise immunity to transient condition.

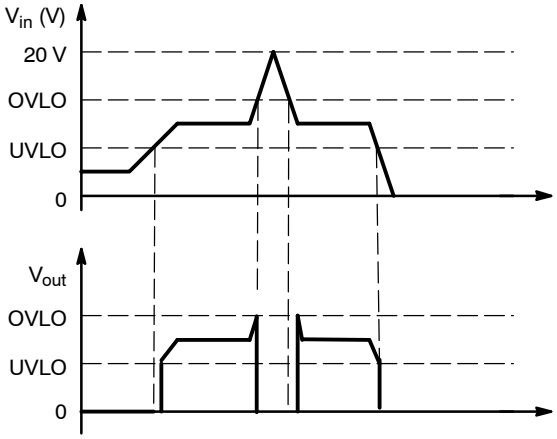


Figure 20. Output Characteristic vs. V_{in}

Overvoltage Lockout (OVLO)

To protect connected systems on V_{out} pin from overvoltage, the device has a built−in overvoltage lock out (OVLO) circuit. During overvoltage condition (OVLO exceeds), the output remains disabled and $\overline{FLAG}$ is tied low, as long as the input voltage is higher than OVLO − hysteresis. This circuit has a 100 mV hysteresis to provide noise immunity to transient conditions.

Overcurrent Protection (OCP)

The NCP361 integrates overcurrent protection to prevent system/battery overload or defect. The current limit threshold is internally set at 750 mA. This value can be changed from 150 mA to 750 mA by a metal tweak, please contact your ON Semiconductor representative for availability. During current fault, the internal PMOS FET is automatically turned off (5 μs) if the charge current exceeds I_{lim}. NCP361 goes into turn on and turn off mode as long as defect is present. The internal ton delay (4 ms typical) allows limiting thermal dissipation. The Flag pin goes to low level when an overcurrent fault appears. That allows the microcontroller to count defect events and turns off the PMOS with EN pin.

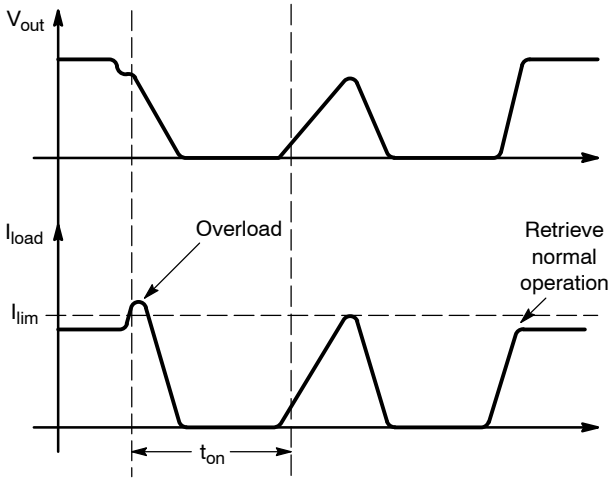


Figure 21. Overcurrent Event Example

$\overline{FLAG}$ Output

NCP361 provides a $\overline{FLAG}$ output, which alerts external systems that a fault has occurred.

This pin is tied to low as soon as: 1.2 V < V_{in} < UVLO, V_{in} > OVLO, I_{charge} > I_{limit}, T_J > 150°C. When NCP361 recovers normal condition, $\overline{FLAG}$ is held high. The pin is an open drain output, thus a pull up resistor (typically 1 MΩ − Minimum 10 kΩ) must be provided to V_{CC}. $\overline{FLAG}$ pin is an open drain output.

$\overline{EN}$ Input

To enable normal operation, the $\overline{EN}$ pin shall be forced to low or connected to ground. A high level on the pin disconnects OUT pin from IN pin. $\overline{EN}$ does not overdrive an OVLO or UVLO fault.

Internal PMOS FET

The NCP361 includes an internal PMOS FET to protect the systems, connected on OUT pin, from positive overvoltage. Regarding electrical characteristics, the $R_{DS(on)}$, during normal operation, will create low losses on V_{out} pin, characterized by V_{in} versus V_{out} dropout.

ESD Tests

The NCP361 fully supports the IEC61000−4−2, level 4 (Input pin, 1 μF mounted on board). That means, in Air condition, V_{in} has a ±15 kV ESD protected input. In Contact condition, V_{in} has ±8 kV ESD protected input. Please refer to Figure 22 to see the IEC61000−4−2 electrostatic discharge waveform.

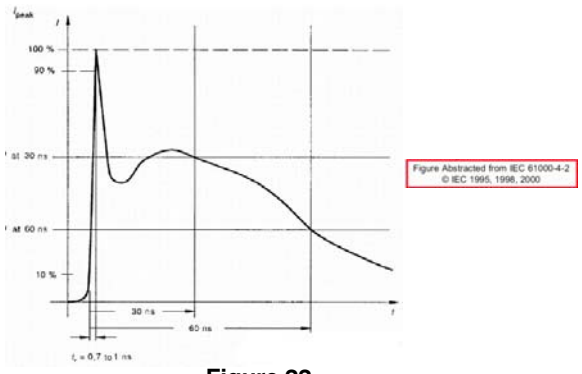


Figure 22.

PCB Recommendations

The NCP361 integrates a 500 mA rated PMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon. The UDFN PAD1 must be connected to ground plane to increase the heat transfer if necessary from an application standpoint. Of course, in any case, this pad shall be not connected to any other potential.

By increasing PCB area, the $R_{\theta JA}$ of the package can be decreased, allowing higher charge current to fill the battery.

Taking into account that internal bondings (wires between package and silicon) can handle up to 1 A (higher than thermal capability), the following calculation shows two different example of current capability, depending on PCB area:

- With 305°C/W (without PCB area), allowing DC current is 500 mA
- With 260°C/W (200 mm^2), the charge DC current allows with a 85°C ambient temperature is:
  $I = \sqrt{(T_J - T_A)/(R_{\theta JA} \times R_{DSON})}$
  I = 625 mA

In every case, we recommend to make thermal measurement on final application board to make sure of the final Thermal Resistance.

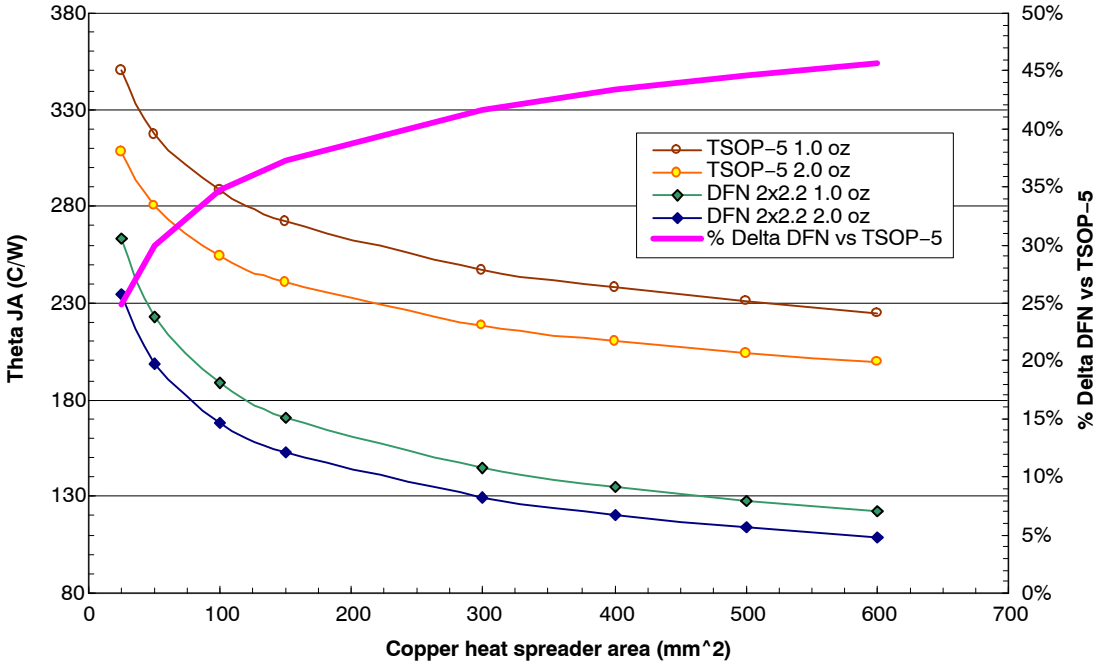


Figure 23. Thermal Resistance of UDFN 2x2 and TSOP Packages as a Function of PCB Area and Thickness

ORDERING INFORMATION

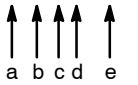
Device	Marking	Package	Shipping†
NCP361MUTBG	AD	UDFN6 (Pb−Free)	3000 / Tape & Reel
NCP361SNT1G	ACD	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV361SNT1G*	VET	TSOP−5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements

SELECTION GUIDE

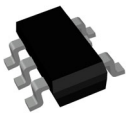
Part number is designated as follows:

NCP361xxxxxTxG



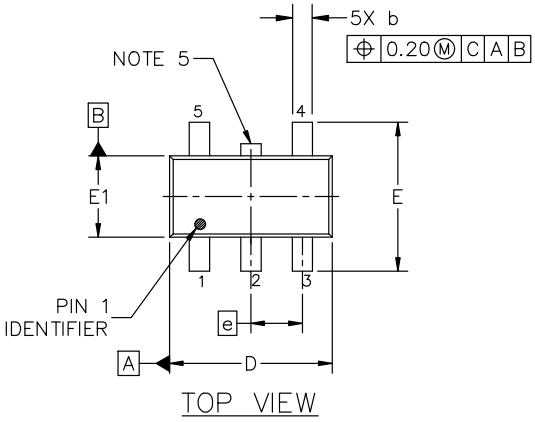
Code	Contents
a	Overcurrent Threshold −: 750 mA
b	Package MU: UDFN SN: TSOP−5
c	UVLO Typical Threshold −: 3.00 V
d	OVLO Typical Threshold −: 5.675 V
e	Tape & Reel Type B: = 3000 1: = 3000

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

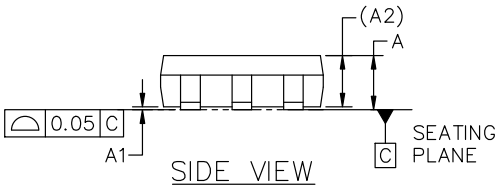


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

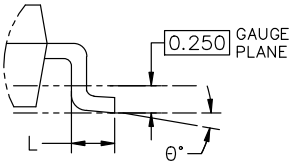
DATE 01 APR 2024



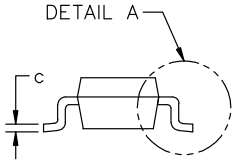
TOP VIEW



SIDE VIEW



DETAIL "A"
SCALE 2:1

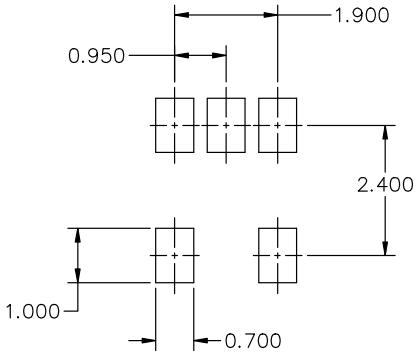


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

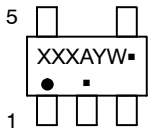
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

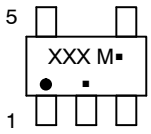
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

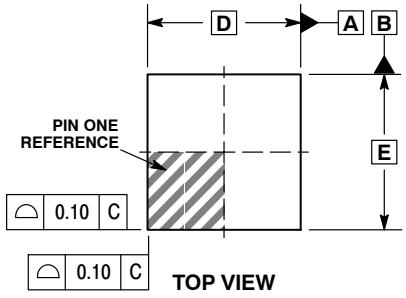
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

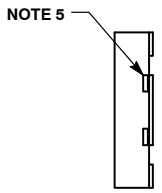
SCALE 4:1

UDFN6 2x2, 0.65P
CASE 517AB
ISSUE C

DATE 10 APR 2013



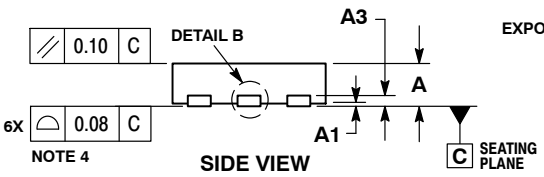
TOP VIEW



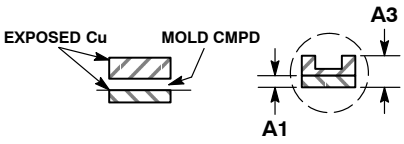
END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
L	0.25	0.35
L1	---	0.15



SIDE VIEW



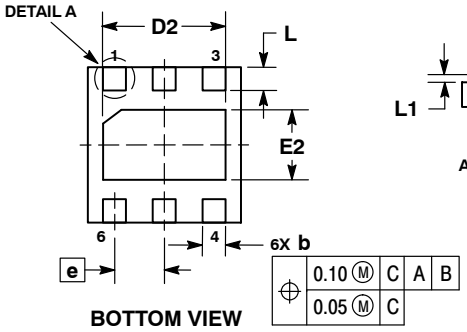
DETAIL B
ALTERNATE
CONSTRUCTIONS

GENERIC
MARKING DIAGRAM*

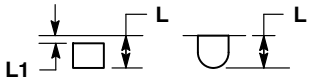
XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

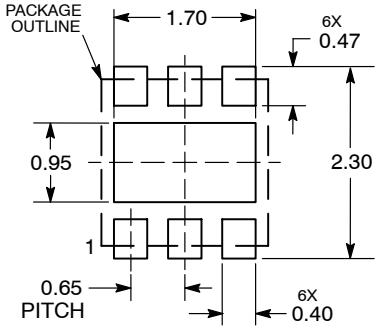


BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

RECOMMENDED
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	UDFN6 2X2, 0.65P	PAGE 1 OF 1

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